GDQ2BFAC

DATASHEET

Features

- Power supply: VDD=VDDQ=1.2V (1.14V~1.26V); VPP=2.5V (2.375V~2.75V)
- JEDEC standard package: 96-Ball FBGA (x16)
- Array Configuration: 8 Banks (x16) 2 groups of 4 banks
- 8n-Bit prefetch architecture
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- Programmable CAS Latency (CL)
- Programmable CAS Write Latency (CWL)
- Internal generated VREF for data inputs
- Data Mask (DM) for write data
- On-Die Termination (ODT): Support Nominal, Park and Dynamic ODT
- Interface: 1.2V Pseudo Open Drain (POD) IO
- Differential clock and data strobe inputs (CK_t ,CK_c; DQS_t, DQS_c)
- Per DRAM Addressability (PDA)
- Data Bus Inversion (DBI)
- Asynchronous reset for power up
- Maximum Power Saving Mode (MPSM)
- Precharge: Auto precharge option for each burst access
- Operating case temperature: -40°C≤T_{CASE}≤95°C
- Support auto-refresh and self-refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Self refresh abort
- Average Refresh Period:
  - 7.8us at -40°C≤T_{CASE}≤85°C
  - 3.9us at 85°C<T_{CASE}≤95°C
- Fine granularity refresh 2x, 4x mode for smaller tRFC
- Programmable data strobe preambles
- Command Address (CA) Parity is supported
- Write Cyclic Redundancy Code (CRC) is supported
- Connectivity test mode (TEN) is supported
- Gear Down Mode
- Output driver calibration through ZQ pin (RZQ: 240Ω±1%)
- Multipurpose register read and write capability
- Write leveling
- Post package repair (PPR)
- JEDEC JESD-79-4D compliant
- RoHS compliant

Note:

1. The functionality described and the timing specifications included in this datasheet are for the DLL Enabled mode of operation (normal operation), unless specifically stated otherwise.

Key Timing Parameters

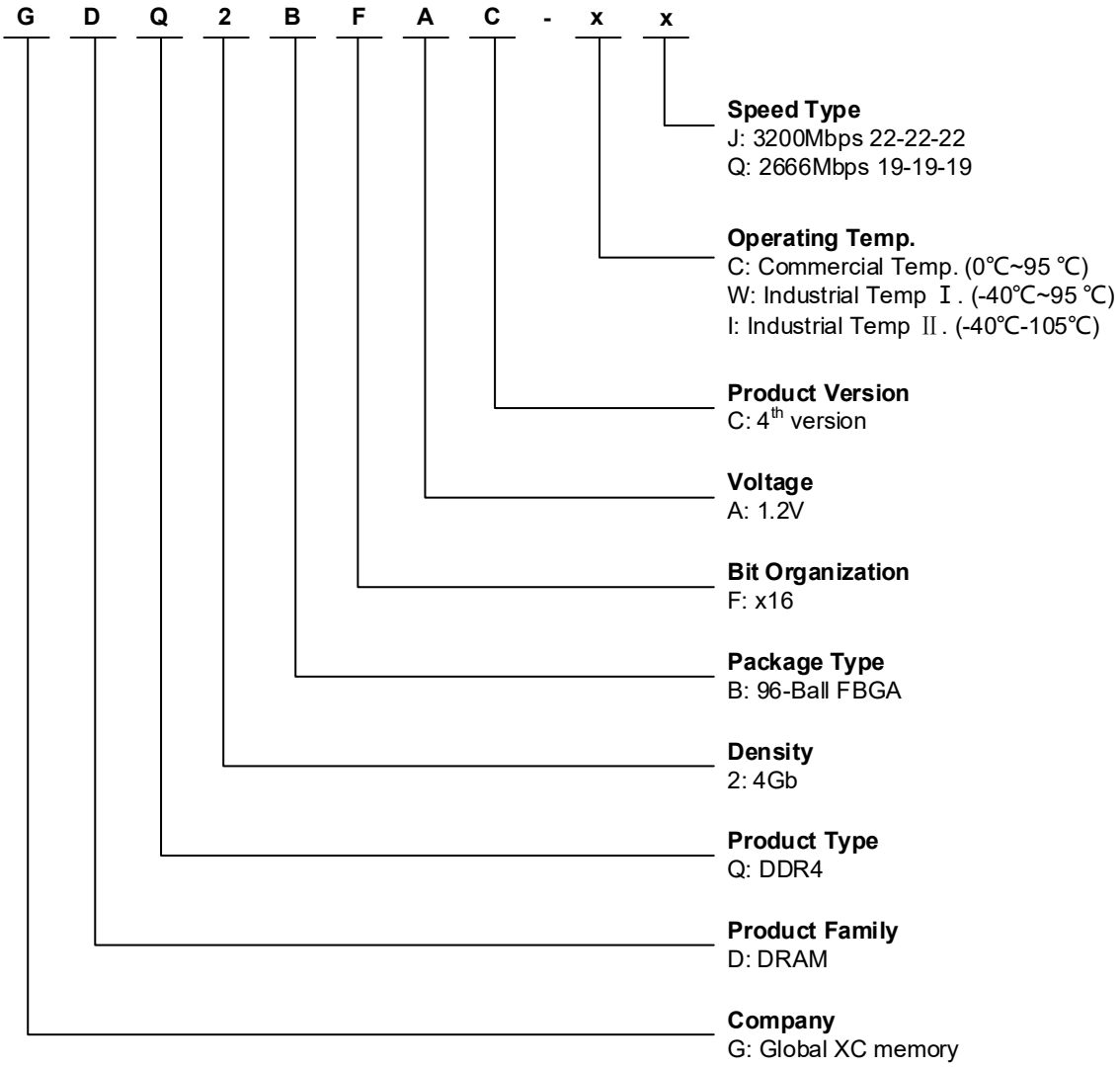
Speed	1600	1866	2133	2400	2666	3200	Unit
CL-t_{RCD}-t_{RP}	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	22-22-22	
tCKmin	1.25	1.071	0.937	0.833	0.75	0.625	ns
CAS Latency	11	13	15	17	19	22	nCK
tRCDmin	13.75	13.92	14.06	14.16	14.25	13.75	ns
tRPmin	13.75	13.92	14.06	14.16	14.25	13.75	ns
tRASmin	35	34	33	32	32	32	ns
tRCmin	48.75	47.92	47.06	46.16	46.25	45.75	ns

Address Table

Parameter	256Mb x16
Number of Bank Groups	2
Number of Banks per Bank Group	4
Bank Group Address	BG0
Bank Address per Bank Group	BA0~BA1
Row Address	A0~A14
Column Address	A0~A9
Page Size	2KB

Ordering Information

Part Number Decoding



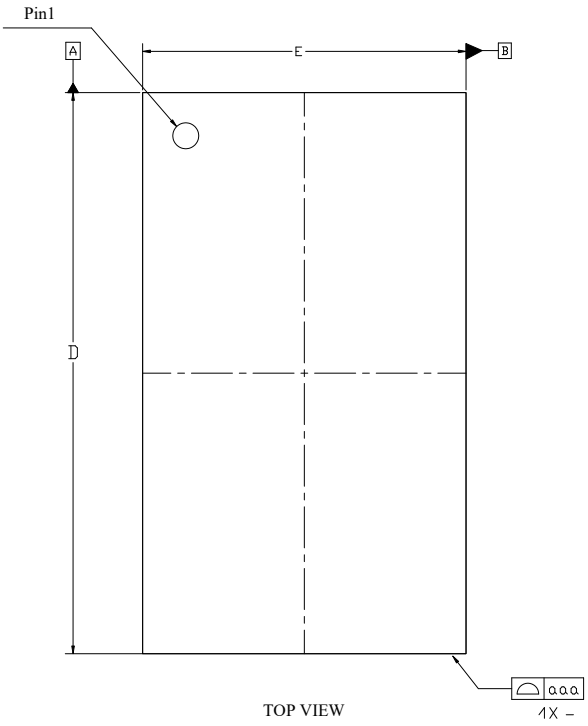
Valid Part Numbers

Part Number	Organization	Data Rate	CL-tRCD-tRP
GDQ2BFAC-CQ	256Mbx16	2666Mbps	19-19-19
GDQ2BFAC-WQ	256Mbx16	2666Mbps	19-19-19
GDQ2BFAC-CJ	256Mbx16	3200Mbps	22-22-22
GDQ2BFAC-WJ	256Mbx16	3200Mbps	22-22-22

Contents

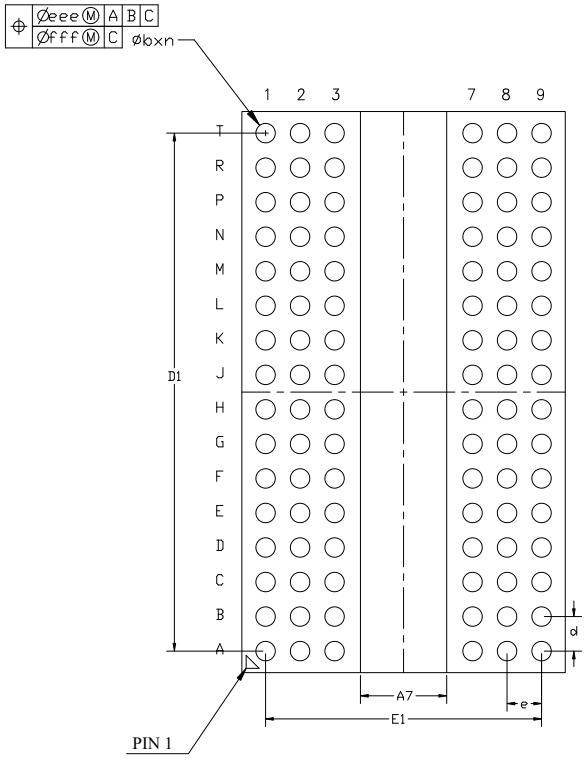
1 Package Information

1.1 Package 96-Ball FBGA (x16)

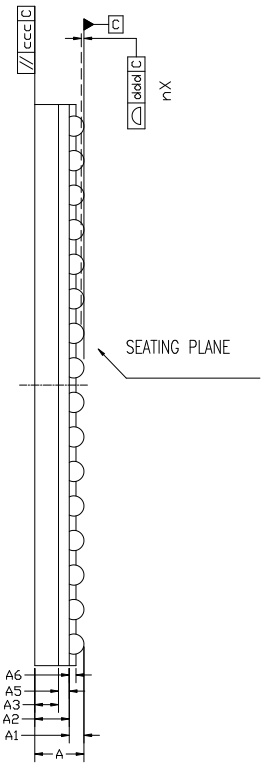


TOP VIEW

	Symbol	Dimension in mm		
		Min	Normal	Max
TOTAL THICKNESS	A	---	1.130	1.200
STAND OFF	A1	0.290	0.340	0.390
SBT+MOLD THICKNESS	A2	0.750	0.790	0.830
MOLD THICKNESS	A3	0.520	0.550	0.580
SUBSTRATE THICKNESS	A5	0.210	0.240	0.270
SLOT THICKNESS	A6	0.105	0.155	0.205
SLOT WIDTH	A7	1.900	2.000	2.100
BALL WIDTH	Φb	0.420	0.470	0.520
BALL PITCH	d	0.800 BASIC		
	e	0.800 BASIC		
BALL COUNT	n	96		
BODY SIZE	D	12.900	13.000	13.100
	E	7.400	7.500	7.600
EDGE BALL CENTER TO CENTER	D1	11.900	12.000	12.100
	E1	6.300	6.400	6.500
PKG EDGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	ccc	0.100		
COPLANARITY	ddd	0.100		
BALL OFFSET(PACKAGE)	eee	0.150		
BALL OFFSET(BALL)	fff	0.080		
JEDEC		MO-207(REF)		



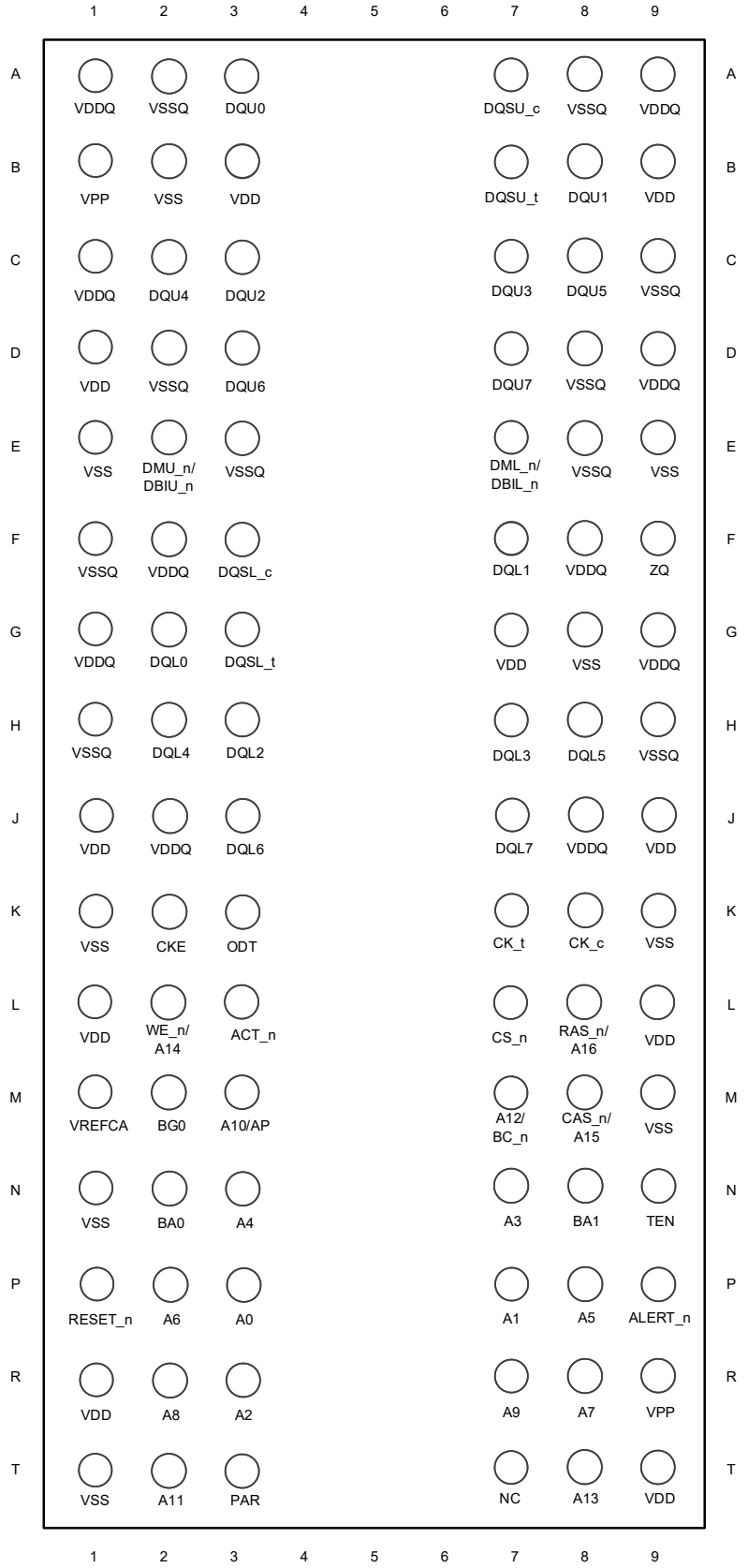
BOTTOM VIEW



SIDE VIEW

2 Ball Assignments

2.1 96-Ball FBGA (x16) Ball Assignments



2.2 Ball Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER- DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). CKE is synchronous for self-refresh exit, however, timing parameters such as tXS are still calculated from the first rising clock edge where CKE HIGH satisfies tIS. After VREFCA and Internal DQ VREF have become stable during the power-on and initialization sequence, they must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during SELF REFRESH.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t and TDQS_c (When TDQS is enabled via Mode Register A11 = 1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation Command Input:** ACT_n defines the ACTIVATION command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/ A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. These balls have multi function. For example, for activation with ACT_n LOW, those are Addressing like A16, A15 and A14 but for non-ACTIVATION command with ACT_n HIGH, those are command pins for READ, WRITE and other command defined in command truth table in JESD79-4D.
DM_n, DBI_n DMU_n/ DBIU_n DML_n/ DBIL_n	I/O	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG[1:0]	Input	**Bank Group Inputs:** BG[1:0] define the bank group to which an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during an MRS cycle. x4/x8 have BG0 and BG1, but x16 has only BG0.
BA[1:0]	Input	**Bank Address Inputs:** BA[1:0] define the bank to which an ACTIVE, READ, WRITE or PRECHARGE command is being applied. Bank address also determines which mode register is to be accessed during an MRS cycle.
A[17:0]	Input	**Address Inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.) The address inputs also provide the op-code during MODE REGISTER SET commands. A17 is only defined for the x4 configuration.
A10/AP	Input	**Auto-precharge:** A10 is sampled during READ/WRITE commands to determine whether Auto-precharge should be performed to the accessed bank after the READ/WRITE operation. (HIGH: Auto-precharge; LOW: No Auto-precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.

Symbol	Type	Function
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See “Command Truth Table” in JESD79-4D.
RESET_n	Input	**Active LOW Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC HIGH and LOW at 80% and 20% of VDD.
DQ DQL, DQU	I/O	**Data Input/Output:** Bi-directional data bus. If CRC is enabled via mode register, then CRC code is added at the end of data burst. Any DQ from DQ3~DQ0 may indicate the internal VREF level during test via mode register setting MR4 A4=HIGH. During this mode, RTT value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	T**ermination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via mode register A11=1 in MR1, the DRAM will enable the same RTT termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When the TDQS function is disabled via mode register A11=0 in MR1, DM/DBI/TDQS pin will provide the Data Mask (DM) function or Data Bus Inversion (DBI) depending on MR5; A11, A12, A10 and TDQS_c is not used. x4/ x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAMs with MR setting. Once it is enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[17:0]. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
ALERT_n	I/O	**Alert:** It has multi functions such as CRC error flag, command and address parity error flag as output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in command address parity check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During connectivity test mode, this pin works as an input. Using this signal or not is dependent on system. In case of not connected as signal, ALERT_n pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. It is required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable connectivity test mode operation along with other pins. It is a CMOS rail to rail signal with AC HIGH and LOW at 80% and 20% of VDD. Using this signal or not is dependent on system. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC	-	**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2V±0.06V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2V±0.06V
VSS	Supply	**Ground**
VPP	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference Voltage for CA
ZQ	Supply	**Reference Pin for ZQ Calibration**

3 Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random-access memory. It is internally configured as an 8-bank (4 banks per Bank Group) DRAM.

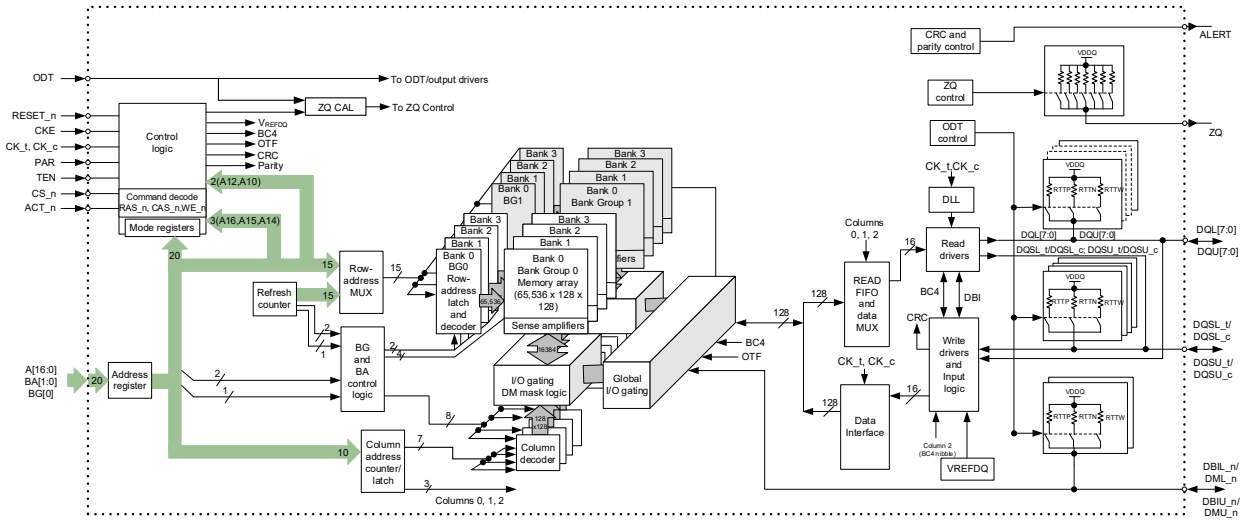


Figure 3-1. 256 Meg x 16 Functional Block Diagram

4 Absolute Maximum Ratings

Table 4-1. Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Note
Voltage on VDD pin relative to VSS	VDD	-0.3	1.5	V	1,3
Voltage on VDDQ pin relative to VSS	VDDQ	-0.3	1.5	V	1,3
Voltage on VPP pin relative to VSS	VPP	-0.3	3.0	V	4
Voltage on any pin except VREFCA relative to VSS	VIN, VOUT	-0.3	1.5	V	1,3,5
Storage temperature	T_{STG}	-55	100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must not be greater than 0.6*VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. VPP must be equal to or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5V is specified in Section 6.3.

5 AC and DC Operating Conditions

5.1 Recommended DC Operating Conditions

Table 5-1. Recommended DC Operating Conditions

Parameter	Symbol	Ratings			Unit	Note
		Min	Typ	Max		
Supply voltage	VDD	1.14	1.2	1.26	V	1,2,3
Supply voltage for output	VDDQ	1.14	1.2	1.26	V	1,2,3
Wordline supply voltage	VPP	2.375	2.5	2.75	V	3

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

5.2 DRAM Component Operating Temperature Range

Table 5-2. Operating Temperature Range

Parameter	Symbol	Rating	Unit	Note
Normal temperature range	T_{OPER}	0~85	°C	1,2
Wide temperature		-40~85	°C	1,2
Extended temperature range		85~95	°C	1,3

Note:

1. Operating temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The normal temperature range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 95°C under all operating conditions for the commercial offering; The wide temperature offerings allow the case temperature to go below 0°C to -40°C.
3. Some applications require operation of the DRAM in the extended temperature range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   - REFRESH commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the extended temperature range. Please refer to the DIMM SPD for option availability.
   - If SELF REFRESH operation is required in the extended temperature range, then it is mandatory to either use the manual self refresh mode with extended temperature range capability (MR2 A6=0 and MR2 A7=1) or enable the optional auto self refresh mode (MR2 A6=1 and MR2 A7=1).

6 AC and DC Input Measurement Levels

6.1 AC and DC Logic Input Levels for Single-Ended Signals

Table 6-1 Single-ended AC and DC Input Levels for Command and Address

Parameter	Symbol	1600/1866/2133/2400		2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
DC input logic HIGH	VIH(DC75)	VREFCA+0.075	VDD	-	-	V	-
DC input logic LOW	VIL(DC75)	VSS	VREFCA-0.075	-	-	V	-
DC input logic HIGH	VIH(DC65)	-	-	VREFCA+0.065	VDD	V	-
DC input logic LOW	VIL(DC65)	-	-	VSS	VREFCA-0.065	V	-
AC input logic HIGH	VIH(AC100)	VREF+0.1	Note2	-	-	V	1
AC input logic LOW	VIL(AC100)	Note2	VREF-0.1	-	-	V	1
AC input logic HIGH	VIH(AC90)	-	-	VREF+0.09	Note2	V	1
AC input logic LOW	VIL(AC90)	-	-	Note2	VREF-0.09	V	1
Reference voltage for ADD, CMD inputs	VREFCA(DC)	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2,3

Note:

1. See “Overshoot/Undershoot Specifications” in Section 6.3.4.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ±1% VDD (for reference: approx.±12mV)
3. For reference: approx. VDD/2±12mV.

6.2 AC and DC Input Measurement Levels: VREF Tolerances

The DC-tolerance limits and AC-noise limits for the reference voltages VREFCA are illustrated in the Figure 6-1 below. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA).

VREF(DC) is the linear average of VREF(t) over a very long period of time (for example, 1 second). This average has to meet the Min/Max requirements in Figure 6-1. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ±1% VDD for the AC-noise limit.

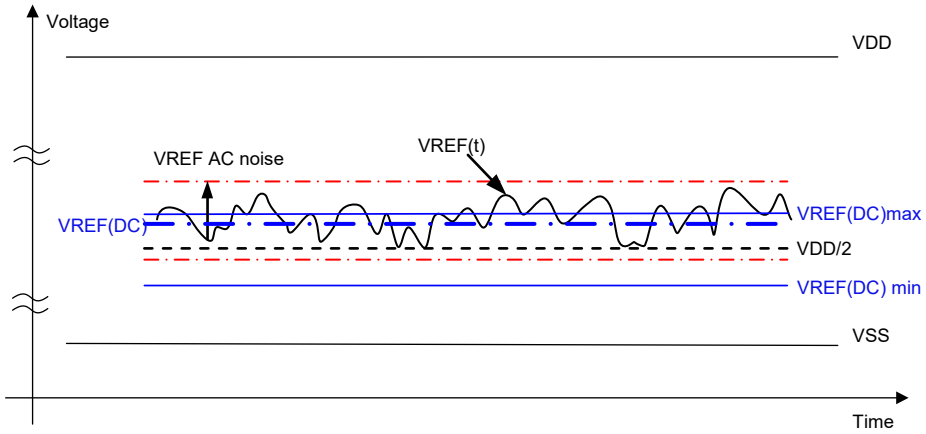


Figure 6-1. Illustration of VREF(DC) Tolerance and VREF AC-noise Limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" should be understood as VREF(DC).

This clarifies that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (±1% of VDD) are included in DRAM timings and their associated deratings.

6.3 AC and DC Logic Input Levels for Differential Signals

6.3.1 AC and DC Logic Input Levels for Differential Signals

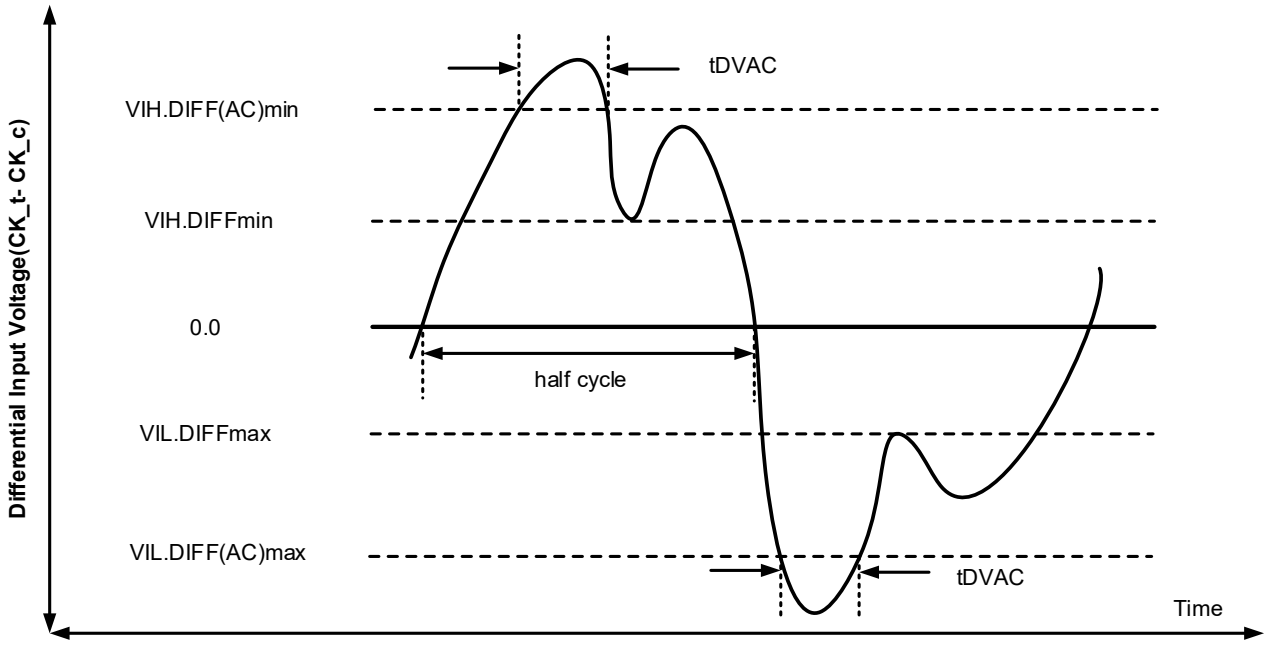


Figure 6-2. Definition of Differential AC-Swing and "Time above AC-Level" tDVAC

Note:

1. Differential signal rising edge from VIL.DIFFmax to VIH.DIFF(AC)min must be monotonic slope.
2. Differential signal falling edge from VIH.DIFFmin to VIL.DIFF(AC)max must be monotonic slope.

6.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

Table 6-2. Differential Input Levels Requirements for CK_t-CK_c

Parameter	Symbol	1600/1866/2133		2400/2666		2933		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Differential input high	VIH.DIFF	+0.150	Note 3	+0.135	Note 3	125	Note 3	+0.110	Note 3	V	1
Differential input low	VIL.DIFF	Note 3	-0.150	Note 3	-0.135	Note 3	-125	Note 3	-0.110	V	1
Differential input high (AC)	VIH.DIFF(AC)	2*(VIH(AC)-VREF)	Note 3	2*(VIH(AC)-VREF)	Note 3	2*(VIH(AC)-VREF)	Note 3	2*(VIH(AC)-VREF)	Note 3	V	2
Differential input low (AC)	VIL.DIFF(AC)	Note 3	2*(VIL(AC)-VREF)	Note 3	2*(VIL(AC)-VREF)	Note 3	2*(VIL(AC)-VREF)	Note 3	2*(VIL(AC)-VREF)	V	2

Note:

1. Used to define a differential signal slew-rate.
2. For CK_t-CK_c use VIH(AC)/VIL(AC) of ADD/CMD and VREFCA.
3. These values are not defined; however, the differential signals (CK_t-CK_c) need to be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 6-3. Allowed Time before Ringback (tDVAC) for CK_t - CK_c

Slew Rate[V/ns]	tDVAC[ps]@|VIHL.DIFF(AC)|=200mV		tDVAC[ps]@|VIHL.DIFF(AC)|=TBDmV	
	Min	Max	Min	Max
>4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
<1.0	80	-	TBD	-

6.3.3 Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin/VSELmax (approximately equal to the AC-levels (VIH(AC)/VIL(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable AC-levels for ADD/CMD might be different per speed-bin etc. E.g., if different value than VIH(AC100) /VIL(AC100) is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK_t and CK_c.

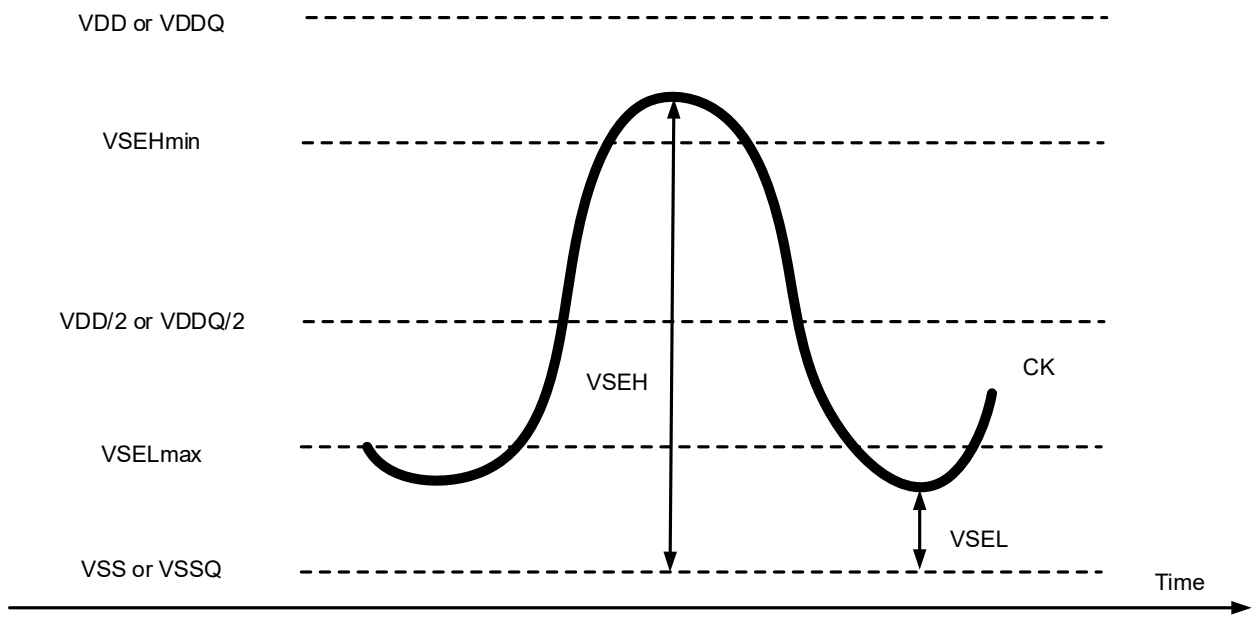


Figure 6-3. Single-Ended Requirement for Differential Signals

Note that, while ADD/CMD signal requirements are with respect to VREFCA, the single-ended components of differential signals have a requirement with respect to VDD/2, this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 6-4. Single-Ended Levels for CK_t, CK_c

Parameter	Symbol	1600/1866/2133		2400/2666		2933/3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
Single-ended high-level for CK_t, CK_c	VSEH	VDD/2+0.100	Note3	VDD/2+0.095	Note3	VDD/2+0.085	Note3	V	1,2
Single-ended low-level for CK_t, CK_c	VSEL	Note3	VDD/2-0.100	Note3	VDD/2-0.095	Note3	VDD/2-0.085	V	1,2

Note:

1. For CK_t-CK_c use VIH(AC) /VIL(AC) of ADD/CMD and VREFCA.
2. VIH(AC)/VIL(AC) for ADD/CMD is based on VREFCA.
3. These values are not defined, however the single-ended signals CK_t, CK_c needs to be within the respective limits (VIH (DC)max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

6.3.4 Address, Command, and Control Overshoot/Undershoot Specifications

Table 6-5. AC Overshoot/Undershoot Specification for Address, Command, and Control Pins

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above VAOS	VAOSP	0.06							V	-
Upper boundary of overshoot area AAOS1	VAOS	VDD+0.24							V	1
Maximum peak amplitude allowed for undershoot area	VAUS	0.30							V	-
Maximum overshoot area per 1 tCK above VAOS	AAOS2	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V-ns	-
Maximum overshoot area per 1 tCK between VDD and VAOS	AAOS1	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V-ns	-
Maximum undershoot area per 1 tCK below VSS	AAUS	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V-ns	-
(A0-A13, BG0, BA0-BA1, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT)										

Note:

1. The value of VAOS matches VDD absolute max as defined in Table 4-1 if VDD equals VDD max as defined in Table 5-1. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 4-1.

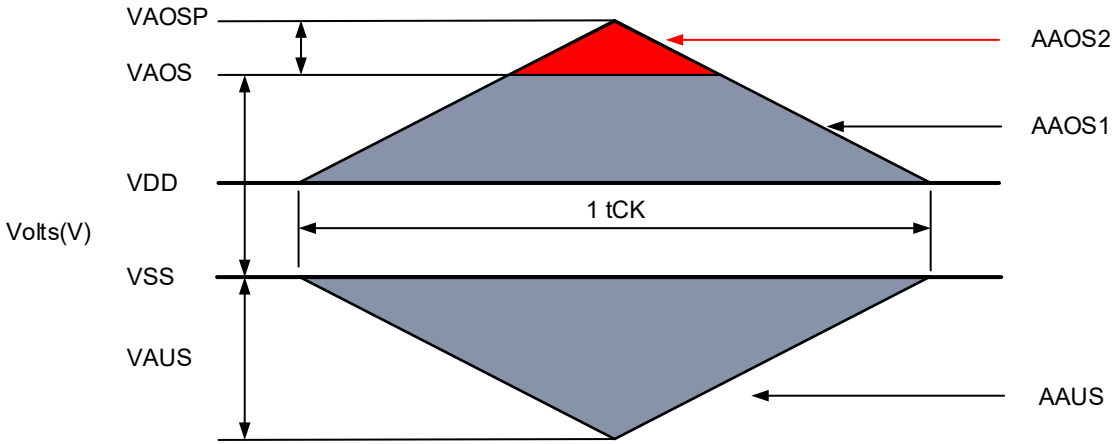


Figure 6-4. Address, Command, and Control Overshoot and Undershoot Definition

6.3.5 Clock Overshoot/Undershoot Specifications

Table 6-6. AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above VCOS	VCOSP	0.06							V	-
Upper boundary of overshoot area ACOS1	VCOS	VDD+0.24							V	1
Maximum peak amplitude allowed for undershoot	VCUS	0.30							V	-
Maximum overshoot area per 1 UI above VCOS	ACOS2	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V-ns	-
Maximum overshoot area per 1 UI between VDD and VCOS	ACOS1	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V-ns	-
Maximum undershoot area per 1 UI below VSS	ACUS	0.1144	0.098	0.0858	0.0762	0.0762	0.0762	0.0762	V-ns	-
(CK_t, CK_c)										

Note:

1. The value of VCOS matches VDD absolute max as defined in Table 4-1 if VDD equals VDD max as defined in Table 5-1. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Table 4-1.

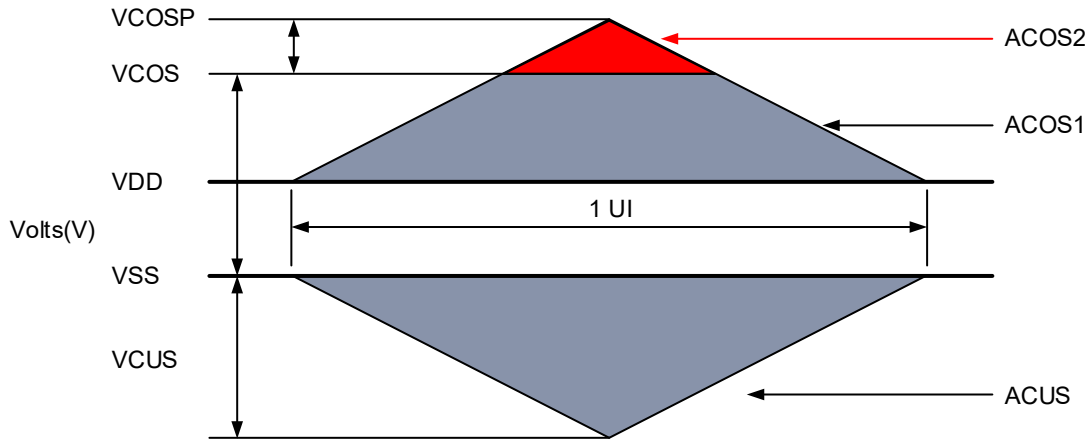


Figure 6-5. Clock Overshoot and Undershoot Definition

6.3.6 Data, Strobe and Mask Overshoot/Undershoot Specifications

Table 6-7. AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above VDOS	VDOSP	0.16							V	-
Upper boundary of overshoot area ADOS1	VDOS	VDD+0.24							V	1
Lower boundary of undershoot area ADUS1	VDUS	0.3							V	2
Maximum peak amplitude below VDUS	VDUSP	0.1							V	-
Maximum overshoot area per UI Above VDOS	ADOS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	-
Maximum overshoot area per 1 UI Between VDDQ and VDOS	ADOS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	-
Maximum undershoot area per 1 UI Between VSSQ and VDUS	ADUS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	-
Maximum undershoot area per 1 UI below VDUS	ADUS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	-
(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)										

Note:

1. The value of VDOS matches (VIN, VOUT) max as defined in Table 4-1 if VDDQ equals VDDQ max as defined Table 5-1. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 4-1.
2. The value of VDUS matches (VIN, VOUT) min as defined in Table 4-1.

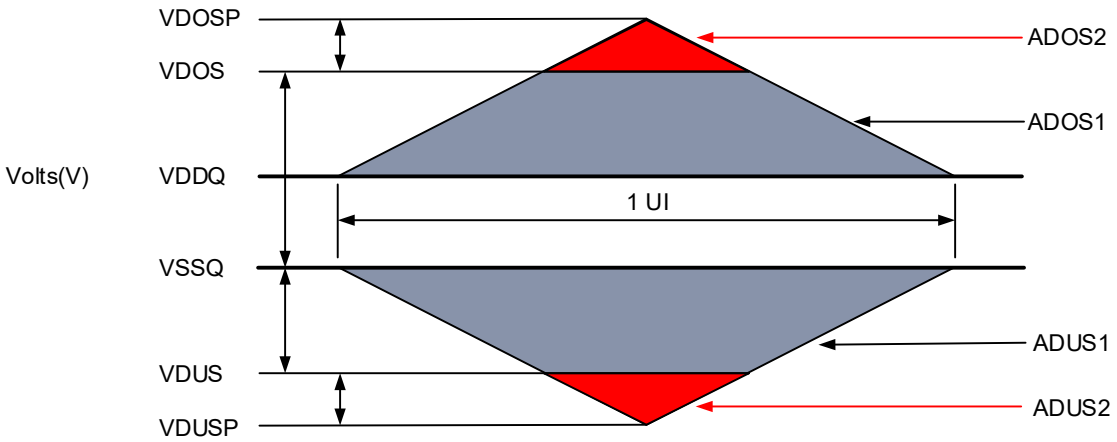


Figure 6-6. Data, Strobe and Mask Overshoot and Undershoot Definition

6.4 Slew Rate Definitions

6.4.1 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 6-8 and Figure 6-7.

Table 6-8. CK Differential Input Slew Rate Definition

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t-CK_c)	VIL.DIFFmax	VIH.DIFFmin	[VIH.DIFFmin-VIL.DIFFmax]/ΔTRdiff
Differential input slew rate for falling edge (CK_t-CK_c)	VIH.DIFFmin	VIL.DIFFmax	[VIH.DIFFmin-VIL.DIFFmax]/ΔTFdiff

Note:

1. The differential signal (i, e., CK_t-CK_c) must be linear between these thresholds.

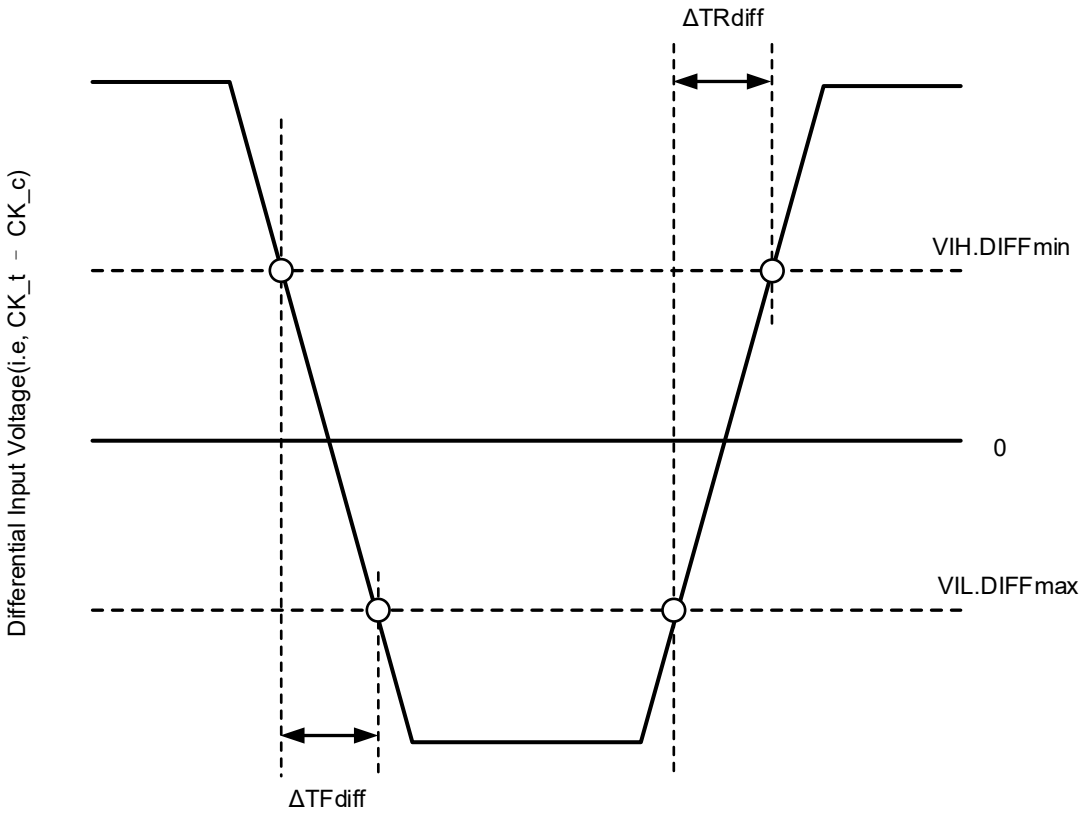


Figure 6-7. Differential Input Slew Rate Definition for CK_t, CK_c

6.4.2 Slew Rate Definitions for Single-Ended Input Signals (CMD/ADD)

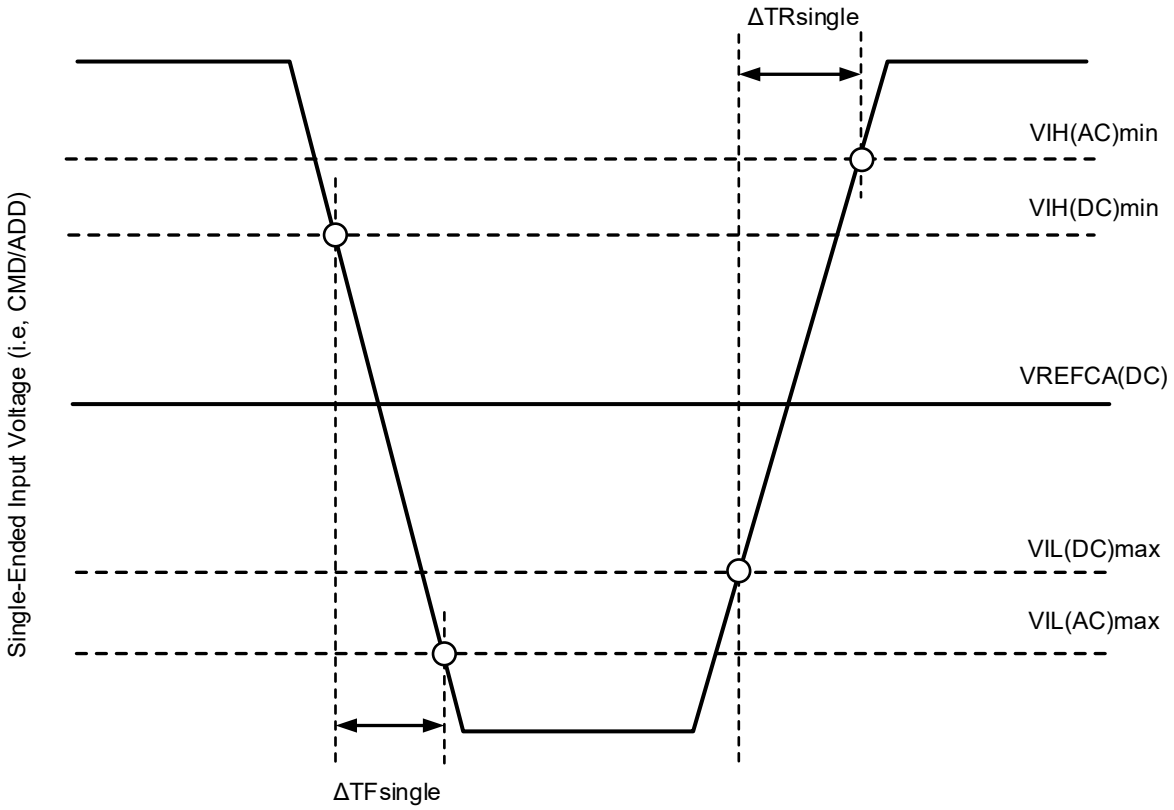


Figure 6-8. Single-Ended Input Slew Rate Definition for CMD and ADD

Note:

1. Single-ended input slew rate for rising edge={VIH(AC)min-VIL(DC)max}/ΔTRse.
2. Single-ended input slew rate for falling edge={VIH(DC)min-VIL(AC)max}/ΔTFse.
3. Single-ended signal rising edge from VIL(DC)max to VIH(DC)min must be monotonic slope.
4. Single-ended signal falling edge from VIH(DC)min to VIL(DC)max must be monotonic slope.

6.5 CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements shown below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

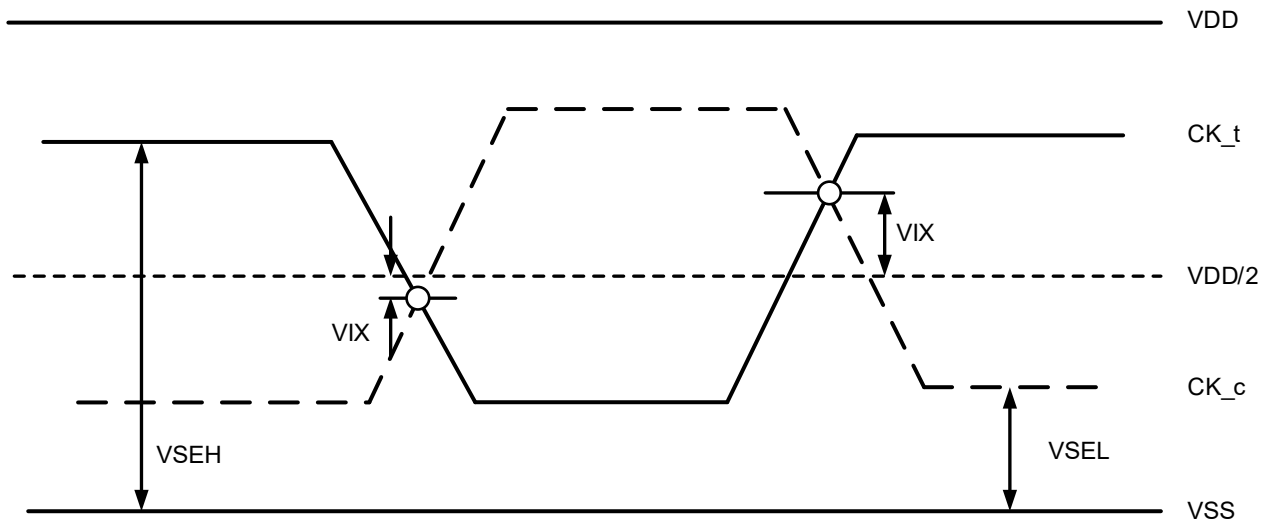


Figure 6-9. VIX Definition (CK)

Table 6-9. Cross Point Voltage for CK Differential Input Signals at DDR4-1666 through DDR4-2400

Parameter	Symbol	Input Level	1666/1866/2133/2400	
			Min	Max
Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VIX_CK	VSEH>VDD/2+145mV	-	120mV
		VDD/2+100mV≤VSEH≤VDD/2+145mV	-	(VSEH-VDD/2)-25mV
		VDD/2-145mV≤VSEL≤VDD/2-100mV	-(VDD/2-VSEL)+25mV	-
		VSEL<VDD/2-145mV	-120mV	-

Table 6-10. Cross Point Voltage for CK Differential Input Signals at DDR4-2666/2933/3200

Parameter	Symbol	Input Level	2666/2933/3200	
			Min	Max
Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VIX_CK	VSEH>VDD/2+145mV	-	110mV
		VDD/2+100mV≤VSEH≤VDD/2+145mV	-	(VSEH-VDD/2)-30mV
		VDD/2-145mV≤VSEL≤VDD/2-90mV	-(VDD/2-VSEL)+30mV	-
		VSEL<VDD/2-145mV	-110mV	-

6.6 CMOS Rail to Rail Input Levels for RESET_n

Table 6-11. CMOS Rail to Rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
Rising Time	TR_RESET	-	1.0	us	4
RESET Pulse Width	tPW_RESET	1.0	-	us	3,5

Note:

1. After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during TPW_RESET, otherwise, the DRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, the DRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal (ringback) requirement during its level transition from LOW to HIGH.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

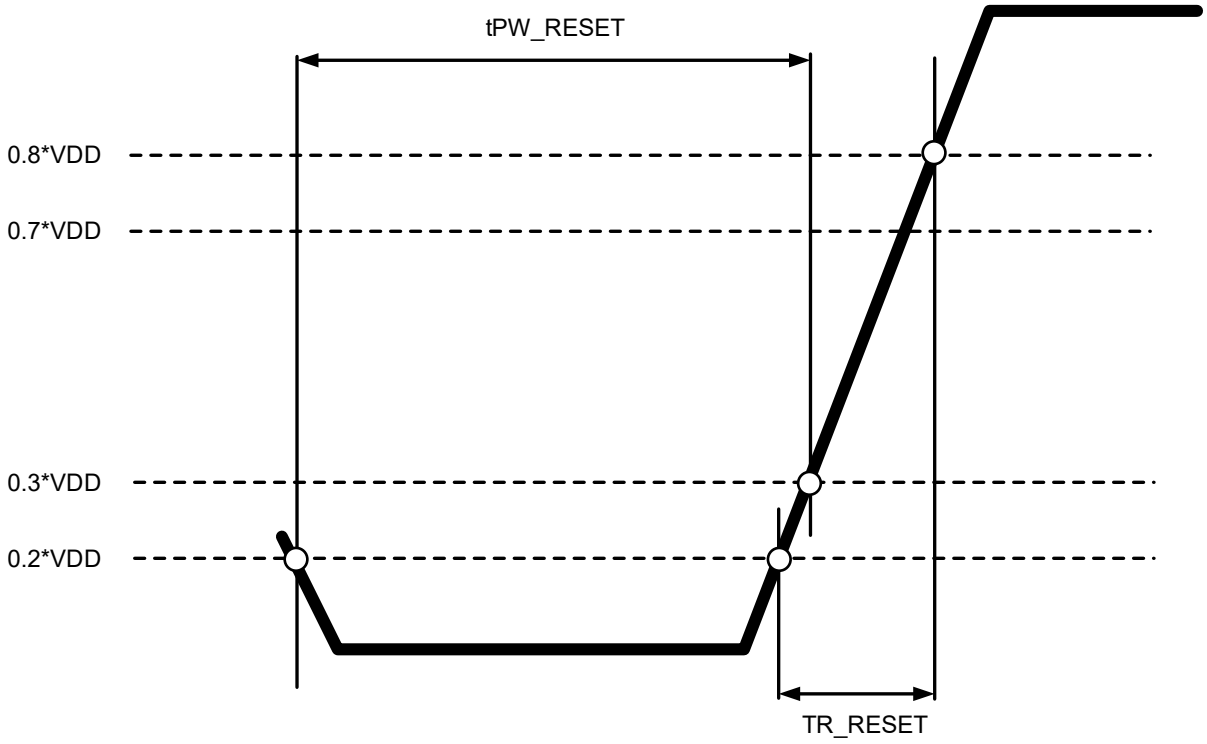


Figure 6-10. RESET_n Input Slew Rate Definition

6.7 AC and DC Logic Input Levels for DQS Signals

6.7.1 Differential Signal Definition

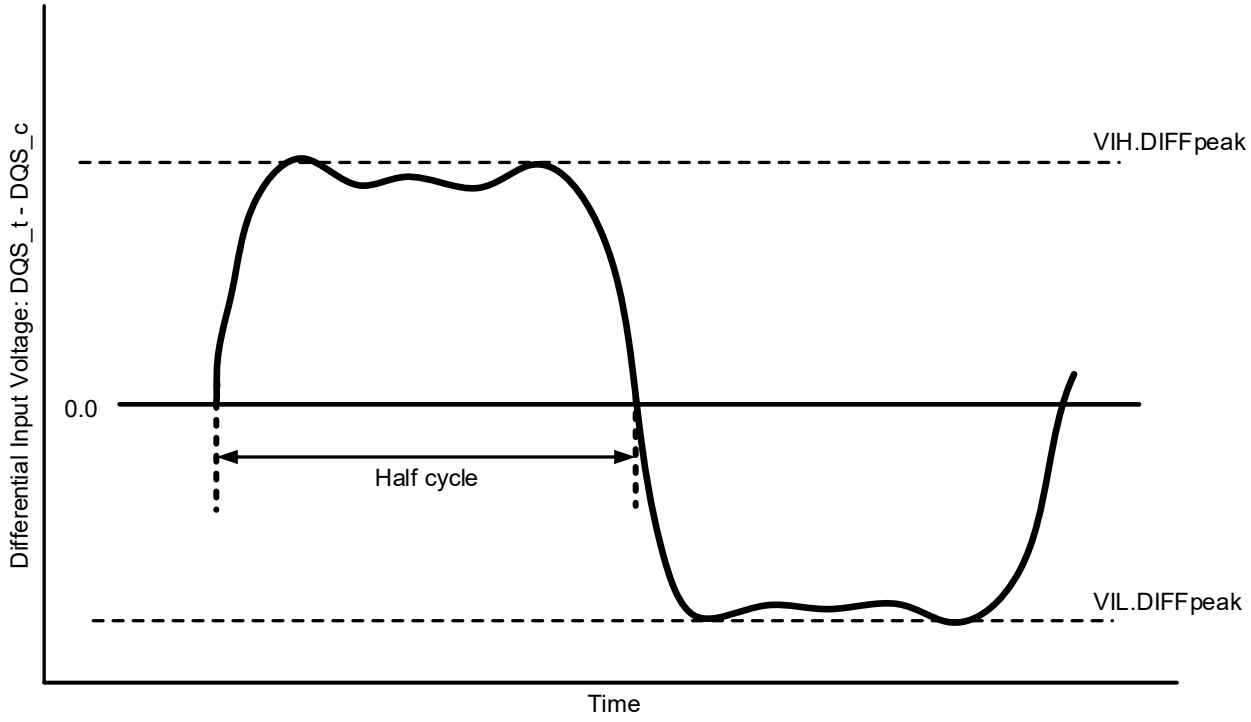


Figure 6-11 Definition of Differential DQS Signal AC-Swing Level

6.7.2 Differential Swing Requirements for DQS (DQS_t - DQS_c)

Table 6-12. Differential Input Swing Requirements for DQS

Parameter	Symbol	1600/1866/2133		2400		2666		2933		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VIH.DIFF.peak Voltage	VIH.DIFFpeak	186	Note2	160	Note2	150	Note2	145	Note2	140	Note2	mV	1
VIL.DIFF.peak Voltage	VIL.DIFFpeak	Note2	-186	Note2	-160	Note2	-150	Note2	-145	Note2	-140	mV	1

Note:

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits of Overshoot, Undershoot Specification for single-ended signals

6.7.3 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated using following equations:

VIH.DIFF.peak voltage=Max(f(t))

VIL.DIFF.peak voltage=Min(f(t))

f(t)=VDQS_t-VDQS_c

The Max(f(t)) or Min(f(t)) used to determine the midpoint from which to reference the ±35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UI's.

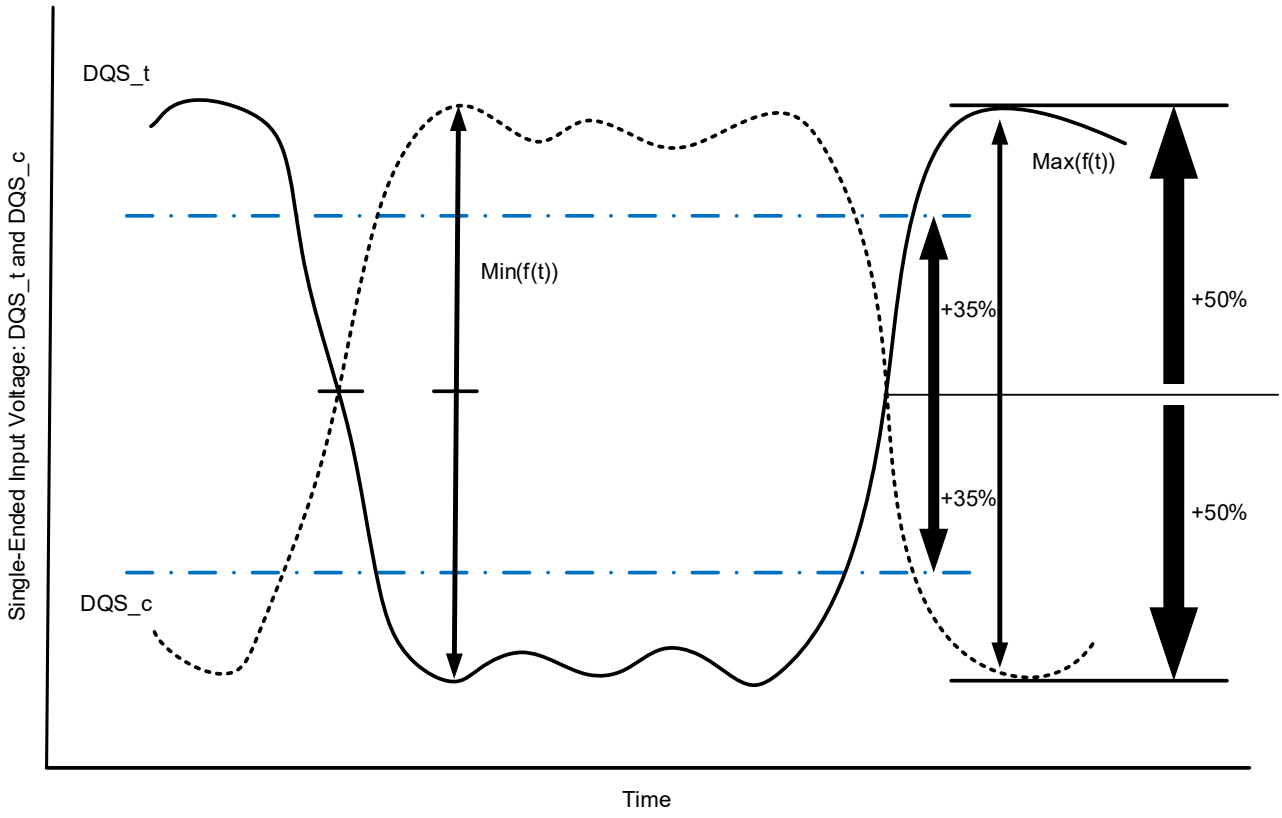


Figure 6-12. Definition of Differential DQS Peak Voltage and Range of Exempt Non-monotonic Signaling

6.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 6-13. The differential input cross point voltage VIX_DQS (VIX_DQS.FR and VIX_DQS.RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQS.mid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQS.mid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within ± 35% of the midpoint of either VIH.DIFF.peak voltage (DQS_t rising) or VIL.DIFF.peak voltage (DQS_c rising), refer to Figure 6-13.

A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 6-13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 6-13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 6-13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 6-13) is not a valid horizontal tangent.

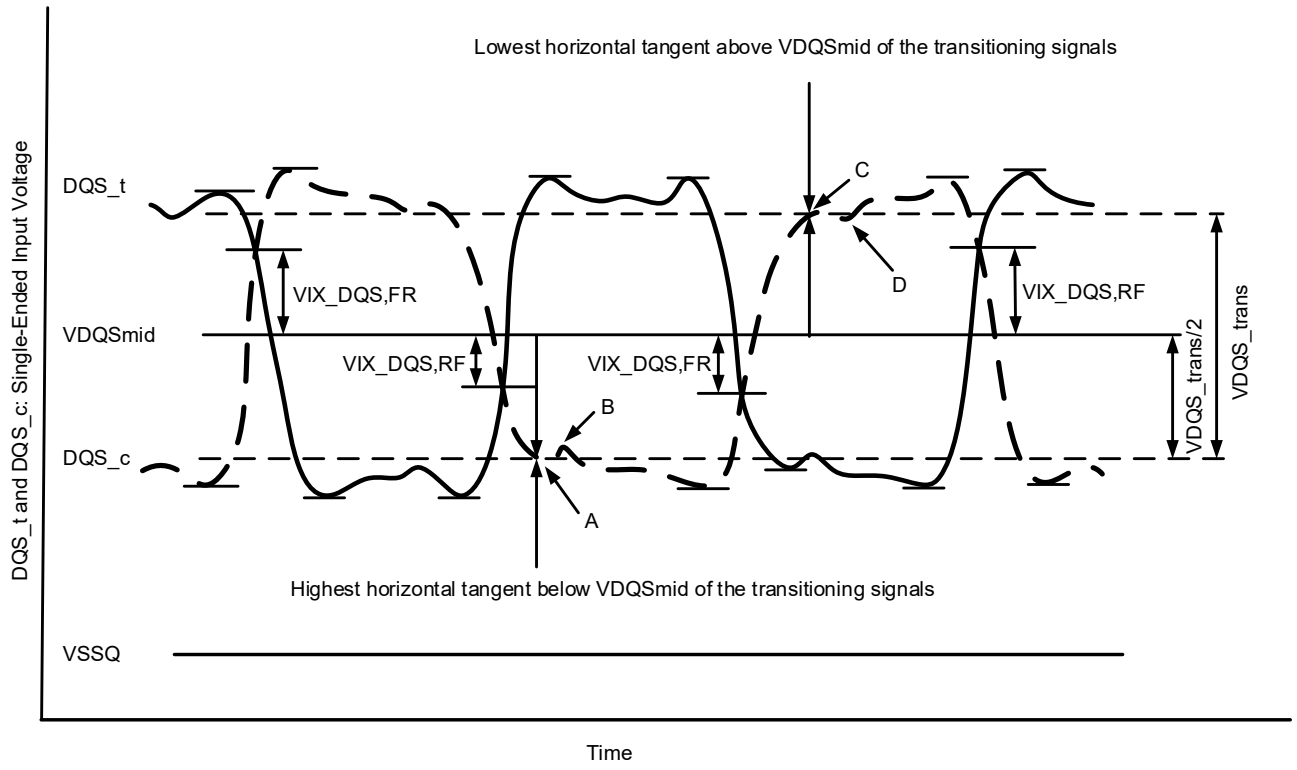


Figure 6-13. VIX Definition (DQS)

Table 6-13. Cross Point Voltage for DQS Differential Input Signals

Parameter	Symbol	1600/1866/2133/2400/2666/2933/3200		Unit	Note
		Min	Max		
DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	VIX_DQSratio	-	25	%	1,2
VDQSmid offset relative to Vcent_DQ(midpoint)	VDQSmid_to_Vcent	-	Note3	mV	3,4,5

Note:

1. VIX_DQSratio is DQS VIX crossing (VIX_DQS.FR or VIX_DQS.RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during VREF Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIH.DIFF_DQS minimum limit or 50mV.
4. VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

6.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 6-14 and Table 6-14.

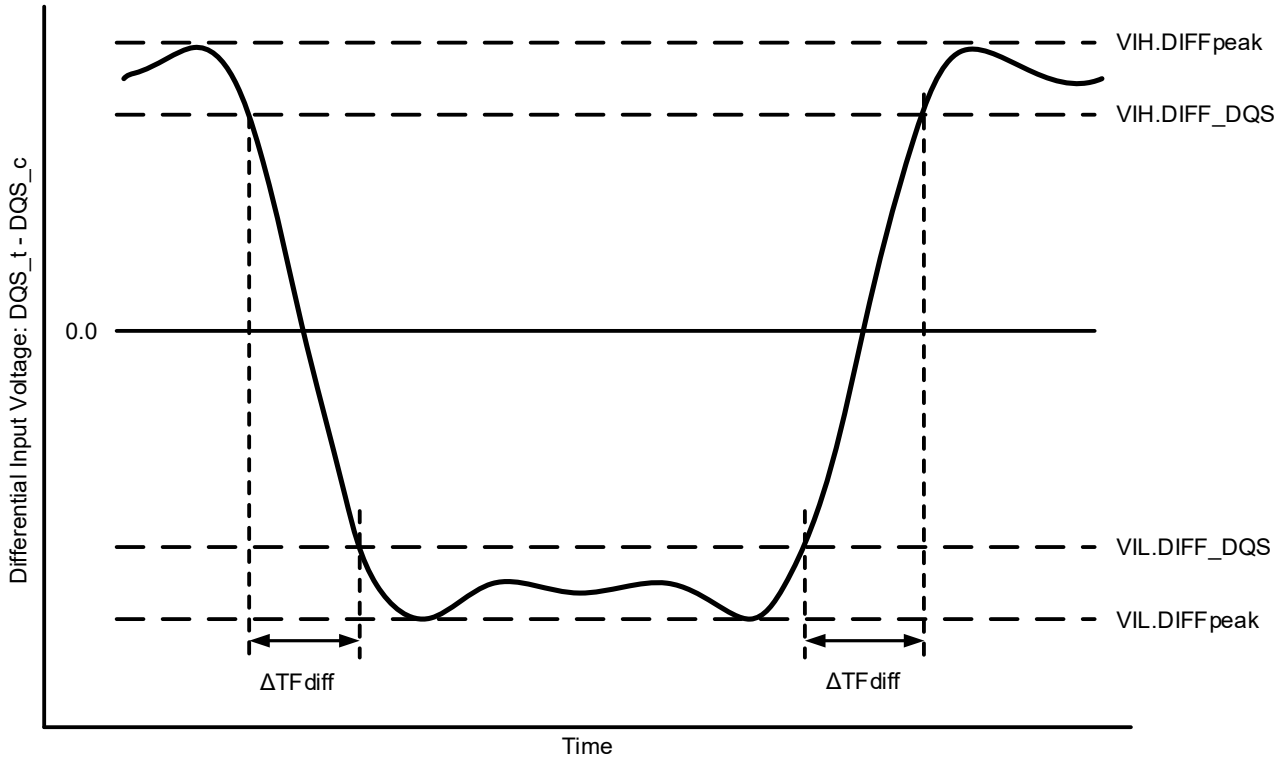


Figure 6-14. Differential Input Slew Rate Definition for DQS_t, DQS_c

Note:

1. Differential signal rising edge from VIL.DIFF_DQS to VIH.DIFF_DQS must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF_DQS to VIL.DIFF_DQS must be monotonic slope.

Table 6-14. Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t-DQS_c)	VIL.DIFF_DQS	VIH.DIFF_DQS	|VIL.DIFF_DQS-VIH.DIFF_DQS|/ΔTRdiff
Differential input slew rate for falling edge (DQS_t-DQS_c)	VIH.DIFF_DQS	VIL.DIFF_DQS	|VIL.DIFF_DQS-VIH.DIFF_DQS|/ΔTFdiff

Table 6-15. Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	1600/1866/2133		2400/2666		2933		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
DC input logic high	VIH.DIFF_DQS	136	-	130	-	115	-	110	-	mV	-
DC input logic low	VIL.DIFF_DQS	-	-136	-	-130	-	-115	-	-110	mV	-

Table 6-16. Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	1600/1866/2133/2400		2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
Differential input slew rate	SRIdiff	3	18	2.5	18	V/ns	-

7 AC and DC Output Measurement Levels

7.1 Output Driver DC Electronic Characteristics

The DDR4 driver supports two different RON values. These RON values are referred as strong (low RON) and weak mode (high RON). A functional representation of the output buffer is shown in Figure 7-1 below. Output driver impedance RON is defined as the individual pull-up and pull-down resistors (RONPu and RONPd).

$RONPu = \frac{VDDQ-VOUT}{|IOUT|}$ under the condition that RONPd is off.

$RONPd = \frac{VOUT}{|IOUT|}$ under the condition that RONPu is off.

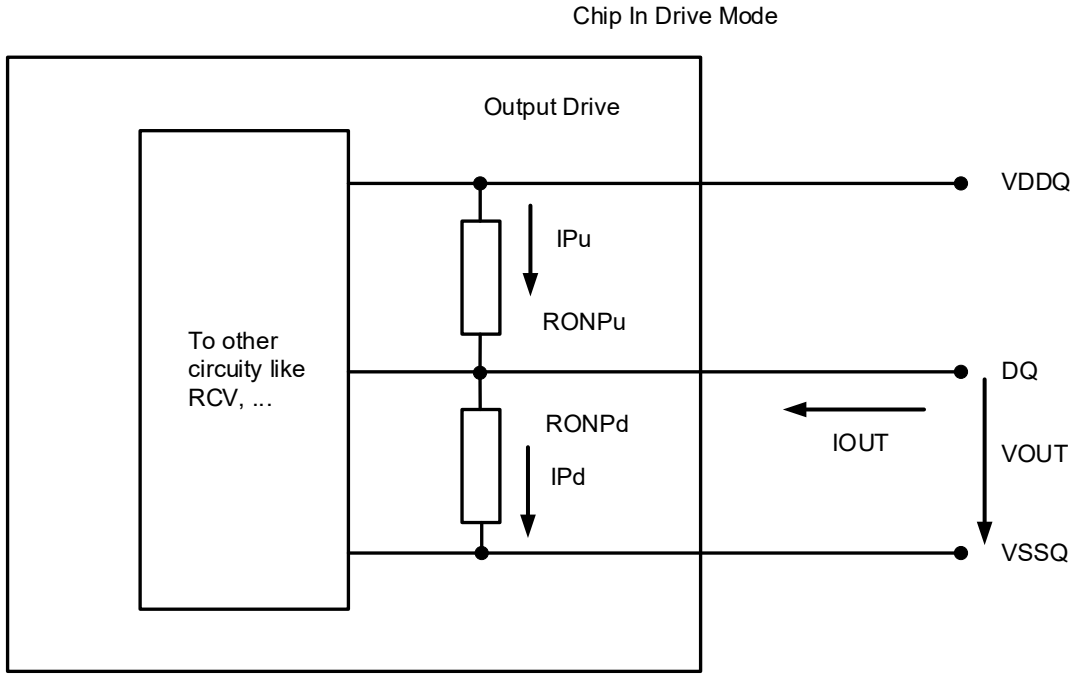


Figure 7-1. Output Driver

Table 7-1. Output Driver DC Electronical Characteristics, Assuming RZQ = 240Ω; Entire Operating Temperature Range; after Proper ZQ Calibration

R_{ONnom}	Resistor	V_{OUT}	Min	Nom	Max	Unit	Note
34Ω	RON34Pd	VOL(DC)=0.5*VDDQ	0.73	1.00	1.10	RZQ/7	1,2
		VOM(DC)=0.8*VDDQ	0.83	1.00	1.10	RZQ/7	1,2
		VOH(DC)=1.1*VDDQ	0.83	1.00	1.25	RZQ/7	1,2
	RON34Pu	VOL(DC)=0.5*VDDQ	0.90	1.00	1.25	RZQ/7	1,2
		VOM(DC)=0.8*VDDQ	0.90	1.00	1.10	RZQ/7	1,2
		VOH(DC)=1.1*VDDQ	0.80	1.00	1.10	RZQ/7	1,2
48Ω	RON48Pd	VOL(DC)=0.5*VDDQ	0.73	1.00	1.10	RZQ/5	1,2
		VOM(DC)=0.8*VDDQ	0.83	1.00	1.10	RZQ/5	1,2
		VOH(DC)=1.1*VDDQ	0.83	1.00	1.25	RZQ/5	1,2
	RON48Pu	VOL(DC)=0.5*VDDQ	0.90	1.00	1.25	RZQ/5	1,2
		VOM(DC)=0.8*VDDQ	0.90	1.00	1.10	RZQ/5	1,2
		VOH(DC)=1.1*VDDQ	0.80	1.00	1.10	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOM(DC)=0.8*VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOM(DC)=0.8*VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-down, MMPddd		VOM(DC)=0.8*VDDQ	-	-	10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd: Measure RONPu and RONPd both at 0.8*VDD separately; RONnom is the nominal RON value.
   MMPuPd=[(RONPu-RONPd)/RONnom]*100
4. RON variance range ratio to RON nominal value in a given component, including DQS_t and DQS_c.
   MMPudd=[(RONPumax-RONPumin)/RONnom]*100
   MMPddd=[(RONPdmax-RONPdmin)/RONnom]*100
5. This parameter of x16 device is specified for upper byte and lower byte.

7.1.1 Alert_n Output Driver Characteristic

A functional representation of the output buffer is shown in Figure 7-2. Output driver impedance RON is defined as follows:

RONPd= $\frac{VOUT}{|IOUT|}$ under the condition that RONPu is off.

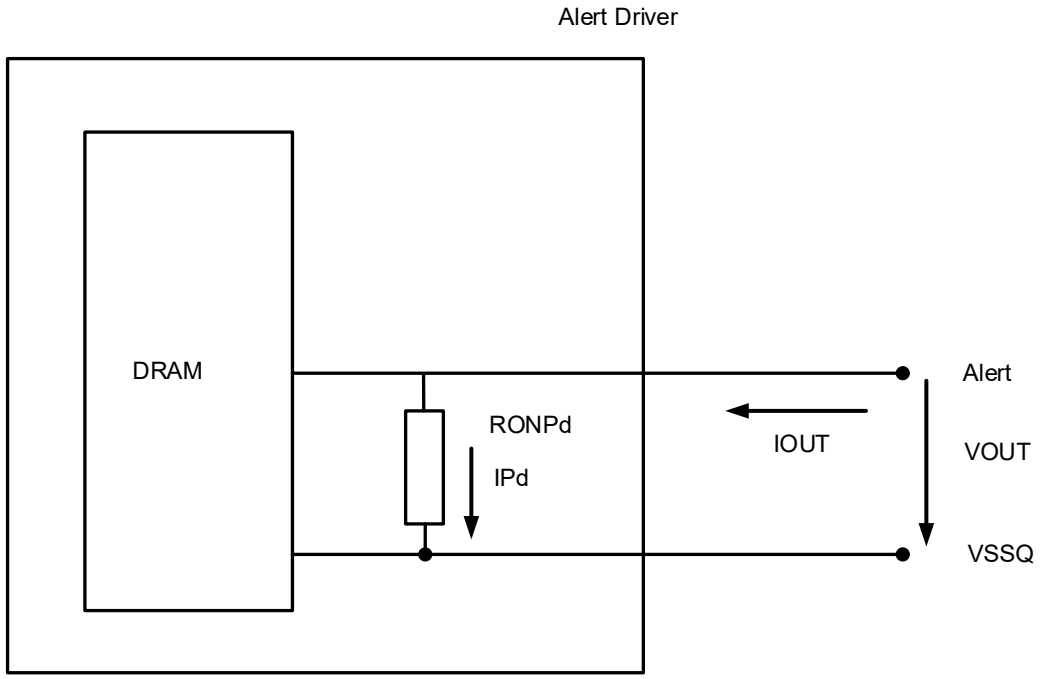


Figure 7-2. Functional Representation of the Output Buffer

Table 7-2. Output Driver Impedance

Resister	VOUT	Min	Max	Unit	Note
RONPd	VOL(DC)=0.1*VDDQ	0.3	1.2	34Ω	1
	VOM(DC)=0.8*VDDQ	0.4	1.2	34Ω	1
	VOH(DC)=1.1*VDDQ	0.4	1.4	34Ω	1

Note:

1. VDDQ voltage is at VDDQ(DC). VDDQ(DC) definition is TBD.

7.1.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

RONPu_CT= $\frac{VDDQ-VOUT}{|IOUT|}$ when RONPd_CT is off.

RONPd_CT= $\frac{VOUT}{|IOUT|}$ when RONPu_CT is off.

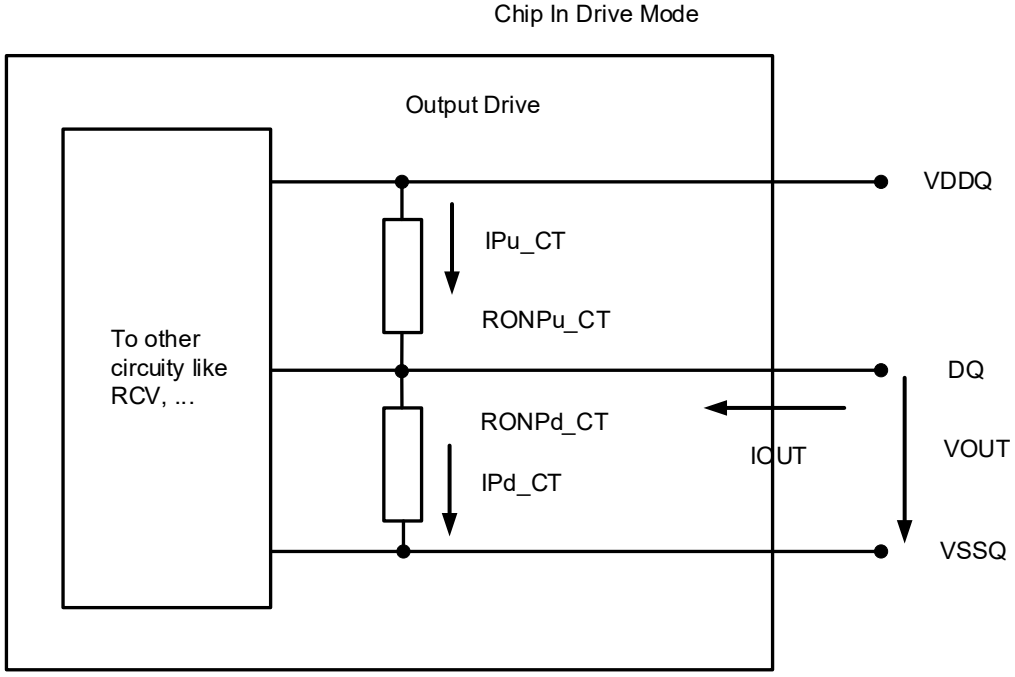


Figure 7-3. Output Driver

Table 7-3. RONPu_CT and RONPd_CT

RONnom_CT	Resister	VOUT	Max	Unit	Note
34Ω	RONPd_CT	VOB(DC)=0.2*VDDQ	1.9	34Ω	1
		VOL(DC)=0.5*VDDQ	2.0	34Ω	1
		VOM(DC)=0.8*VDDQ	2.2	34Ω	1
		VOH(DC)=1.1*VDDQ	2.5	34Ω	1
	RONPu_CT	VOB(DC)=0.2*VDDQ	2.5	34Ω	1
		VOL(DC)=0.5*VDDQ	2.2	34Ω	1
		VOM(DC)=0.8*VDDQ	2.0	34Ω	1
		VOH(DC)=1.1*VDDQ	1.9	34Ω	1

Note:

1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

7.2 Single-Ended AC and DC Output Levels

Table 7-4. Single-ended AC and DC Output Levels

Parameter	Symbol	1600 to 3200	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)	1.1*VDDQ	V	-
DC output mid measurement level (for IV curve linearity)	VOM(DC)	0.8*VDDQ	V	-
DC output low measurement level (for IV curve linearity)	VOL(DC)	0.5*VDDQ	V	-
AC output high measurement level (for output SR)	VOH(AC)	(0.7+0.15)*VDDQ	V	1
AC output low measurement level (for output SR)	VOL(AC)	(0.7-0.15)*VDDQ	V	1

Note:

1. The swing of ±0.15*VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to VTT=VDDQ.

7.3 Differential AC&DC Output Levels

Table 7-5. Differential AC&DC Output Levels

Parameter	Symbol	1600 to 3200	Unit	Note
AC differential output high measurement level (for output SR)	VOH.DIFF(AC)	+0.3*VDDQ	V	1
AC differential output low measurement level (for output SR)	VOL.DIFF(AC)	-0.3*VDDQ	V	1

Note:

1. The swing of ±0.3*VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT=VDDQ at each of the differential outputs.

7.4 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals as shown in Table 7-6 and Figure 7-3.

Table 7-6. Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)]/ΔTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)]/ΔTFse

Note:

1. Output slew rate is verified by designed and characterization, and may not be subject to production test.

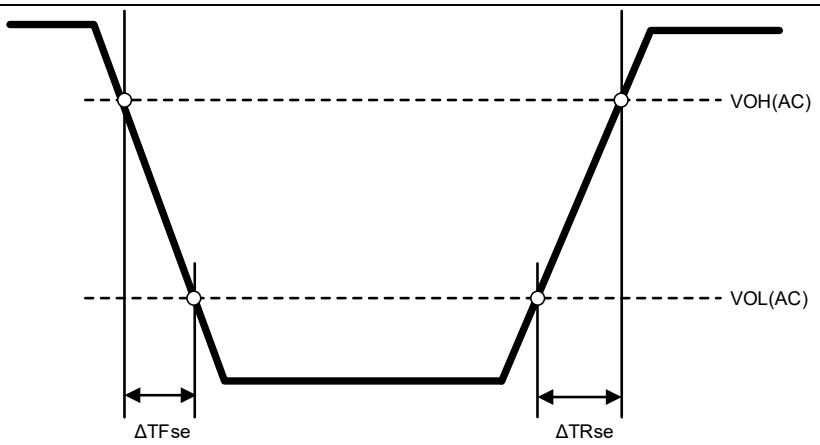


Figure 7-4. Single-ended Output Slew Rate Definition

Table 7-7. Single-ended Output Slew Rate

Parameter	Symbol	1600 to 3200		Unit	Note
		Min	Max		
Single-ended output slew rate	SRQse	4	9	V/ns	1

Description:

SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Singnals; For RON = RZQ/7 setting.

Note:

1. In two cases, a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane.
   - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from LOW to HIGH or HIGH to LOW respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9V/ns applies.

7.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 7-8 and Figure 7-4.

Table 7-8. Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOL.DIFF(AC)	VOH.DIFF(AC)	[VOH.DIFF(AC)-VOL.DIFF(AC)]/ΔTRdiff
Differential output slew rate for falling edge	VOH.DIFF(AC)	VOL.DIFF(AC)	[VOH.DIFF(AC)-VOL.DIFF(AC)]/ΔTFdiff

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

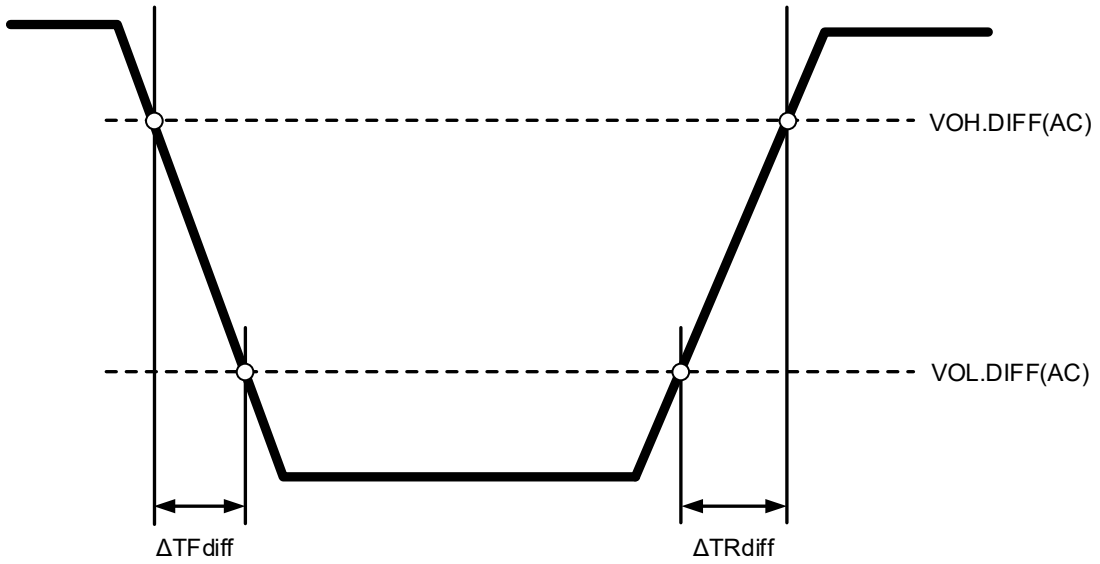


Figure 7-5. Differential Output Slew Rate Definition

Table 7-9. Differential Output Slew Rate

Parameter	Symbol	1600 to 3200		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	18	V/ns

Description:

SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output);

Diff: Differential Singnals; For RON=RZQ/7 setting.

7.6 Single-Ended AC& DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Table 7-10. Single-Ended AC&DC Output Level of Connectivity Test Mode

Parameter	Symbol	1600 to 3200	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)	1.1*VDDQ	V	-
DC output mid measurement level (for IV curve linearity)	VOM(DC)	0.8*VDDQ	V	-
DC output low measurement level (for IV curve linearity)	VOL(DC)	0.5*VDDQ	V	-
DC output below measurement level (for IV curve linearity)	VOB(DC)	0.2*VDDQ	V	-
AC output high measurement level (for output SR)	VOH(AC)	VTT+(0.1*VDDQ)	V	1
AC output below measurement level (for output SR)	VOL(AC)	VTT-(0.1*VDDQ)	V	1

Note:

1. The effective test load is 50Ω terminated by VTT=0.5*VDDQ.

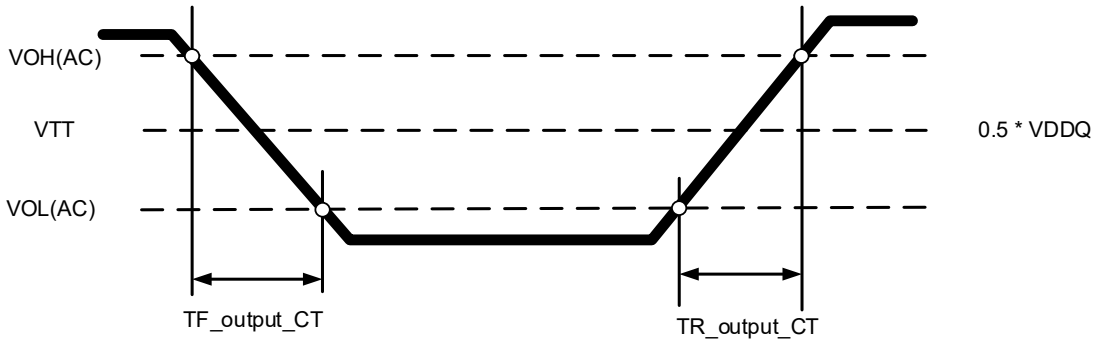


Figure 7-6. Output Slew Rate Definition of Connectivity Test Mode

Table 7-11. Single-Ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	1600 to 3200		Unit	Note
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	-
Output signal Rising time	TR_output_CT	-	10	ns/V	-

7.7 Reference Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 7-7.

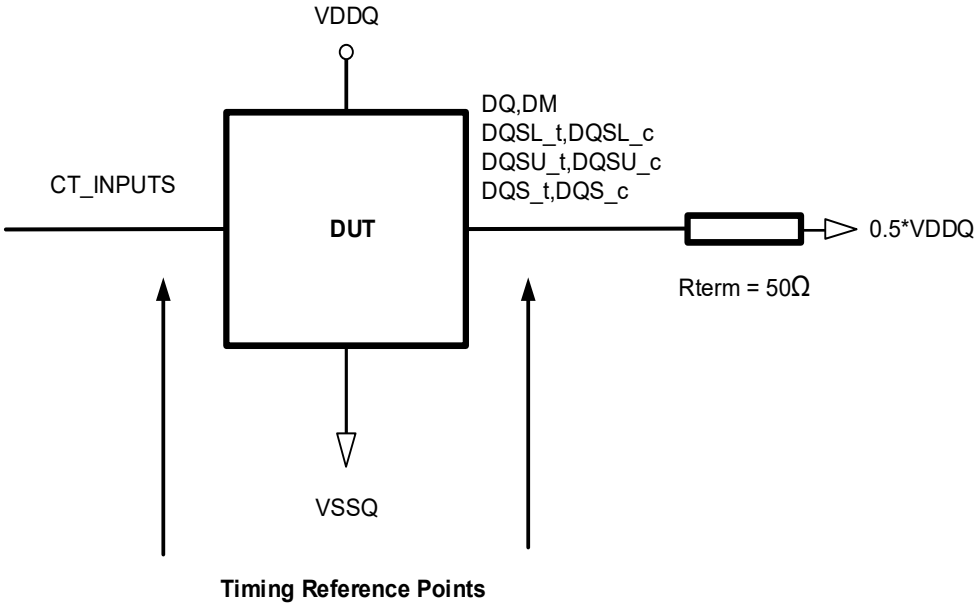


Figure 7-7. Connectivity Test Mode Timing Reference Load

8 Speed Bin

8.1 DDR4-2400 Speed Bins and Operations

Table 8-1. DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	Note
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal READ command to first data			tAA	14.16 (13.75)(9)	18.00	ns	9
Internal READ command to first data with Read DBI enabled			tAA_DBI	tAAmin+3nCK	tAAmax+3nCK	ns	9
ACT to internal READ or WRITE delay time			tRCD	14.16 (13.75)(9)	-	ns	9
PRE command period			tRP	14.16 (13.75)(9)	-	ns	9
ACT to PRE command period			tRAS	32	9*tREFI	ns	9
ACT to ACT or REF command period			tRC	46.16 (45.75)(9)	-	ns	9
	Normal	READ DBI					
CWL=9	CL=9	CL=11	tCK(avg)	Reserved		ns	4
	CL=10	CL=12	tCK(avg)	1.5	1.6	ns	1,2,3,4,5,8
CWL=9,11	CL=10	CL=12	tCK(avg)	Reserved		ns	4
	CL=11	CL=13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,5
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,5
CWL=10,12	CL=12	CL=14	tCK(avg)	Reserved		ns	4
	CL=13	CL=15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,5
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,5
CWL=11,14	CL=14	CL=17	tCK(avg)	Reserved		ns	4
	CL=15	CL=18	tCK(avg)	0.937	<1.071	ns	1,2,3,4,5
	CL=16	CL=19	tCK(avg)	0.937	<1.071	ns	1,2,3,5
CWL=12,16	CL=15	CL=18	tCK(avg)	Reserved		ns	4
	CL=16	CL=19	tCK(avg)	Reserved		ns	4
	CL=17	CL=20	tCK(avg)	0.833	<0.937	ns	1,2,3,4
	CL=18	CL=21	tCK(avg)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,17,18		nCK	10
Supported CL Settings with READ DBI				12,(13),14,(15),16,(18),19,20,21		nCK	10
Supported CWL Settings				9,10,11,12,14,16		nCK	-

8.2 DDR4-2666 Speed Bins and Operations

Table 8-2. DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	Note
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal READ command to first data			tAA	14.25 (13.75)(9)	18.00	ns	9
Internal READ command to first data with Read DBI enabled			tAA_DBI	tAAmin+3nCK	tAAmax+3nCK	ns	9
ACT to internal READ or WRITE delay time			tRCD	14.25 (13.75)(9)	-	ns	9
PRE command period			tRP	14.25 (13.75)(9)	-	ns	9
ACT to PRE command period			tRAS	32	9*tREFI	ns	9
ACT to ACT or REF command period			tRC	46.25 (45.75)(9)	-	ns	9
	Normal	READ DBI					
CWL=9	CL=9	CL=11	tCK(avg)	Reserved		ns	4
	CL=10	CL=12	tCK(avg)	1.5	1.6	ns	1,2,3,6,8
CWL=9,11	CL=10	CL=12	tCK(avg)	Reserved		ns	4
	CL=11	CL=13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,6
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,6
CWL=10,12	CL=12	CL=14	tCK(avg)	Reserved		ns	4
	CL=13	CL=15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,6
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,6
CWL=11,14	CL=14	CL=17	tCK(avg)	Reserved		ns	4
	CL=15	CL=18	tCK(avg)	0.937	<1.071	ns	1,2,3,4,6
	CL=16	CL=19	tCK(avg)	0.937	<1.071	ns	1,2,3,6
CWL=12,16	CL=15	CL=18	tCK(avg)	Reserved		ns	4
	CL=16	CL=19	tCK(avg)	Reserved		ns	4
	CL=17	CL=20	tCK(avg)	0.833	<0.937	ns	1,2,3,4,6
	CL=18	CL=21	tCK(avg)	0.833	<0.937	ns	1,2,3,6
CWL=14,18	CL=17	CL=20	tCK(avg)	Reserved		ns	4
	CL=18	CL=21	tCK(avg)	Reserved		ns	4
	CL=19	CL=22	tCK(avg)	0.75	<0.833	ns	1,2,3,4
	CL=20	CL=23	tCK(avg)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	10
Supported CL Settings with READ DBI				12,(13),14,(15),16,(18),19,(20),21,22,23		nCK	10
Supported CWL Settings				9,10,11,12,14,16,18		nCK	-

8.3 DDR4-3200 Speed Bins and Operations

Table 8-3. DDR4-3200 Speed Bins and Operations

Speed Bin				3200		Unit	Note
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	Min	Max		
Internal READ command to first data			tAA	13.75	18.00	ns	9
Internal READ command to first data with READ DBI enabled			tAA_DBI	tAAmin+4nCK	tAAmax+4nCK	ns	9
ACT to internal Read or Write delay time			tRCD	13.75	-	ns	9
PRE command period			tRP	13.75	-	ns	9
ACT to PRE command period			tRAS	32	9*tREFI	ns	9
ACT to ACT or REF command period			tRC	45.75	-	ns	9
	Normal	Read DBI					
CWL=9	CL=9	CL=11	tCK(avg)	Reserved		ns	4
	CL=10	CL=12	tCK(avg)	1.5	1.6	ns	1,2,3,7,8
CWL=9,11	CL=10	CL=12	tCK(avg)	Reserved		ns	4
	CL=11	CL=13	tCK(avg)	1.25	<1.5	ns	1,2,3,4,7
	CL=12	CL=14	tCK(avg)	1.25	<1.5	ns	1,2,3,7
CWL=10,12	CL=12	CL=14	tCK(avg)	Reserved		ns	4
	CL=13	CL=15	tCK(avg)	1.071	<1.25	ns	1,2,3,4,7
	CL=14	CL=16	tCK(avg)	1.071	<1.25	ns	1,2,3,7
CWL=11,14	CL=14	CL=17	tCK(avg)	Reserved		ns	4
	CL=15	CL=18	tCK(avg)	0.937	<1.071	ns	1,2,3,4,7
	CL=16	CL=19	tCK(avg)	0.937	<1.071	ns	1,2,3,7
CWL=12,16	CL=15	CL=18	tCK(avg)	Reserved		ns	4
	CL=16	CL=19	tCK(avg)	Reserved		ns	4
	CL=17	CL=20	tCK(avg)	0.833	<0.937	ns	1,2,3,4,7
	CL=18	CL=21	tCK(avg)	0.833	<0.937	ns	1,2,3,7
CWL=14,18	CL=17	CL=20	tCK(avg)	Reserved		ns	4
	CL=18	CL=21	tCK(avg)	Reserved		ns	4
	CL=19	CL=22	tCK(avg)	0.75	<0.833	ns	1,2,3,4,7
	CL=20	CL=23	tCK(avg)	0.75	<0.833	ns	1,2,3,7
CWL=16,20	CL=20	CL=24	tCK(avg)	Reserved		ns	4
	CL=21	CL=25	tCK(avg)	0.682	<0.75	ns	1,2,3,4,7
	CL=22	CL=26	tCK(avg)	0.682	<0.75	ns	1,2,3,7
	CL=24	CL=28	tCK(avg)	0.682	<0.75	ns	1,2,3,7
CWL=16,20	CL=20	CL=24	tCK(avg)	Reserved		ns	4
	CL=22	CL=26	tCK(avg)	0.625	<0.682	ns	1,2,3,4
	CL=24	CL=28	tCK(avg)	0.625	<0.682	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22,24		nCK	-
Supported CL Settings with READ DBI				12,13,14,15,16,18,19,20,21,22,23,25,26,28		nCK	-
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	-

Speed Bin Table Note

Absolute Specifications

- VDDQ=VDD=1.20V±0.06V
- VPP=2.5V(2.375Vmin,2.75Vmax)
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when gear down mode is disabled.

1. The CL setting and CWL setting result in tCK(avg)min and tCK(avg)max requirements. When selecting tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg)min limits: Since CAS latency is not purely analog - data and strobe output are synchronized by the DLL- all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in JEDEC-79D Section 13.5.
3. tCK(avg)max limits: Calculate tCK(avg) = tAAmax/CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg)max corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
6. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
7. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
8. DDR4-1600 AC timing apply if DRAM operates at lower than 1600MT/s data rate.
9. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
10. CL number in parentheses, it means that these numbers are optional.
11. DDR4 SDRAM supports CL=9 as long as a system meets tAAmin, tRCDmin, tRPmin, and tRCmin.
12. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

8.4 tREFI and tRFC Parameters

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 8-4. t_{REFI} and t_{RFC} Parameters

Refresh Mode	Parameter		4Gb	Unit
	tREFI(base)		7.8	us
1x mode	tREFI1	-40°C≤T_{CASE}≤85°C	tREFI(base)	us
		85°C<T_{CASE}≤95°C	tREFI(base)/2	us
	tRFC1		260	ns
2x mode	tREFI2	-40°C≤T_{CASE}≤85°C	tREFI(base)/2	us
		85°C<T_{CASE}≤95°C	tREFI(base)/4	us
	tRFC2		160	ns
4x mode	tREFI4	-40°C≤T_{CASE}≤85°C	tREFI(base)/4	us
		85°C<T_{CASE}≤95°C	tREFI(base)/8	us
	tRFC4		110	ns

9 IDD and IDDQ Specification Parameters and Test Conditions

9.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 9-1 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate I/O power of the DDR4 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in Figure 9-2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN≤VIL(AC)max.
- “1” and “HIGH” is defined as VIN≥VIH(AC)min.
- “MID-LEVEL” is defined as inputs are VREF=VDD/2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 9-1.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 9-2.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 9-3 to Table 9-11.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting:
  RON=RZQ/7 (34Ω in MR1);
  RTT_NOM=RZQ/6 (40Ω in MR1);
  RTT_WR=RZQ/2 (120Ω in MR2);
  RTT_PARK=Disable;
  Qoff=0B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3;
  READ/WRITE DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement can be taken.
- Define D={CS_n, ACT_n, RAS_n, CAS_n, WE_n}:={HIGH, LOW, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D#={CS_n, ACT_n, RAS_n, CAS_n, WE_n}:={HIGH, HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

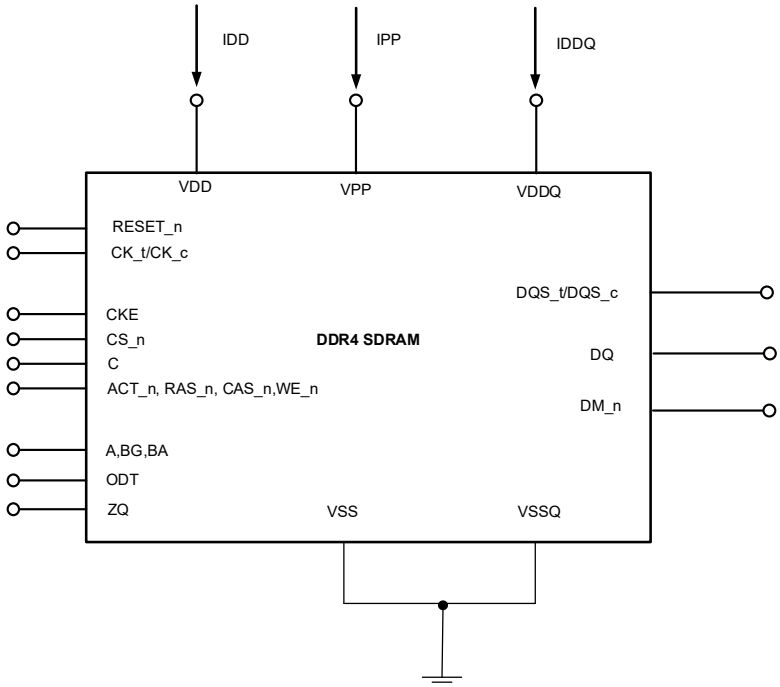


Figure 9-1. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

Note:

1. DIMM level Output test load condition may be different from above

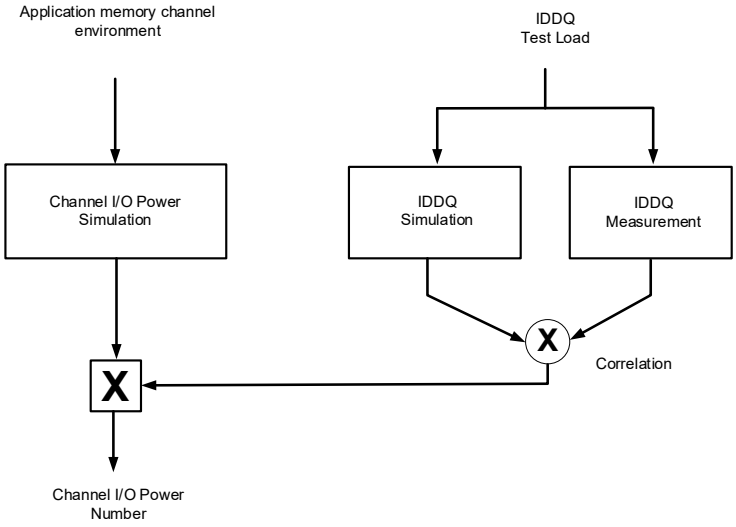


Figure 9-2. Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

Table 9-1. Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		1600	1866	2133	2400	2666	2933	3200	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK		1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CL		11	13	15	17	19	21	22	nCK
CWL		11	12	14	16	18	20	20	nCK
nRCD		11	13	15	17	19	21	22	nCK
nRC		39	45	51	56	62	68	74	nCK
nRAS		28	32	36	39	43	47	52	nCK
nRP		11	13	15	17	19	21	22	nCK
nFAW	x8	20	22	23	26	28	31	34	nCK
	x16	28	28	32	36	40	44	48	nCK
nRRDS	x8	4	4	4	4	4	4	4	nCK
	x16	5	6	6	7	8	8	9	nCK
nRRDL	x8	5	5	6	6	7	8	8	nCK
	x16	6	6	7	8	9	10	11	nCK
tCCD_S		4	4	4	4	4	4	4	nCK
tCCD_L		5	5	6	6	7	8	8	nCK
tWTR_S		2	3	3	3	4	4	4	nCK
tWTR_L		6	7	8	9	10	11	12	nCK
nRFC 2Gb		128	150	171	193	214	235	256	nCK
nRFC 4Gb		208	243	278	313	347	382	416	nCK
nRFC 8Gb		280	327	374	421	467	514	560	nCK

Table 9-2. Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL = 0)** **CKE:** HIGH; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n:** HIGH between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-3. **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see Table 9-3); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-3.
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL=CL-1, Other conditions:** See IDD0.
IPP0	**Operating One Bank Active-Precharge IPP Current (AL=0)** Same condition with IDD0.
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** HIGH; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: HIGH between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data I/O:** Partially toggling according to Table 9-4 **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see Table 9-4); **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-4.
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL=CL-1, Other conditions**: See IDD1.
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** Same condition with IDD1.
IDD2N	**Precharge Standby Current (AL=0)** **CKE:** HIGH; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-5. **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-5.
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL=CL-1, Other conditions:** See IDD2N.
IPP2N	**Precharge Standby IPP Current** Same condition with IDD2N.

Symbol	Description
IDD2NT	**Precharge Standby ODT Current** **CKE:** HIGH; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-6. **Data I/O:** VSSQ; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Toggling according toTable 9-6; **Pattern Details:** See Table 9-6.
IDDQ2NT	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current.
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled(3).
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled(3),(5).
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled(3) .
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled(3) .
IDD2P	**Precharge Power-Down Current** **CKE:** LOW; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
IPP2P	**Precharge Power-Down IPP Current** Same condition with IDD2P.
IDD2Q	**Precharge Quiet Standby Current** **CKE**: HIGH; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
IDD3N	**Active Standby Current (AL=0)** **CKE:** HIGH; **External clock:** On; **tCK, CL:** see Table 9-1; **BL:** 8(1);

Symbol	Description
	AL: 0; **CS_n:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-5. **Data I/O**: VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-5.
IDD3NA	**Active Standby Current (AL=CL-1)** **AL=CL-1, Other conditions:** See IDD3N
IPP3N	**Active Standby IPP Current** Same condition with IDD3N.
IDD3P	**Active Power-Down Current** **CKE:** LOW; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks open; **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
IPP3P	**Active Power-Down IPP Current** Same condition with IDD3P.
IDD4R	**Operating Burst Read Current** **CKE:** HIGH; **External clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n**: HIGH between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-7. **Data I/O**: Seamless read data burst with different data between one burst and the next one according to Table 9-7. **DM_n:** Stable at 1; **Bank Activity:** All banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see Table 9-7) **Output Buffer and RTT**: Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-7.
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL=CL-1, Other conditions:** See IDD4R.
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled(3), Other conditions:** See IDD4R.
IPP4R	**Operating Burst Read IPP Current** Same condition with IDD4R.
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current.
IDDQ4RB	**Operating Burst Read IDDQ Current with READ DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current.
IDD4W	**Operating Burst Write Current** **CKE:** HIGH;

Symbol	Description
	External clock: On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n:** HIGH between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-8; **Data I/O**: Seamless write data burst with different data between one burst and the next one according to Table 9-8 **DM_n:** Stable at 1; **Bank Activity:** All banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (Table 9-8); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at HIGH; **Pattern Details:** See Table 9-8.
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL=CL-1, Other conditions:** See IDD4W.
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled(3), Other conditions:** See IDD4W.
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled(3), Other conditions:** See IDD4W.
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled(3), Other conditions:** See IDD4W.
IPP4W	**Operating Burst Write IPP Current** Same condition with IDD4W.
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** HIGH; **External clock:** On; **tCK, CL nRFC:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n:** HIGH between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-10. **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** REF command every nRFC (see Table 9-10); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details**: See Table 9-10.
IPP5B	**Burst Refresh Write IPP Current (1X REF)** Same condition with IDD5B.
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC*2, Other conditions:** See IDD5B.
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** Same condition with IDD5F2.
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC*4, Other conditions:** See IDD5B.
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** Same condition with IDD5F4.
IDD6N	**Self Refresh Current: Normal Temperature Range** **T_{CASE} for CT devices:** 0°C~85°C, **T_{CASE} for IT devices:** -40°C~85°C; **Low Power Auto Self Refresh (LP ASR)**: Normal(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 9-1; **BL:** 8(1);

Symbol	Description
	AL: 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n:** Stable at 1; **Bank Activity:** SELF REFRESH operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** Same condition with IDD6N.
IDD6E	**Self Refresh Current: Extended Temperature Range** **T_{CASE} for CT devices:** 0°C~95°C, **T_{CASE} for IT devices:** -40°C~95°C; **Low Power Auto Self Refresh (LP ASR)**: Extended(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 9-1; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Extended Temperature SELF REFRESH operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** Same condition with IDD6E.
IDD6R	**Self Refresh Current: Reduced Temperature Range** **T_{CASE} for CT devices:** 0°C~45°C, **T_{CASE} for IT devices:** -40°C~45°C; **Low Power Auto Self Refresh (LP ASR)**: Reduced(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 9-1; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Extended Temperature SELF REFRESH operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** Same condition with IDD6R.
IDD6A	**Auto Self Refresh Current** **T_{CASE} for CT devices:** 0°C~95°C, **T_{CASE} for IT devices:** -40°C~95°C; **Low Power Auto Self Refresh (LP ASR)**: Auto(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 9-1; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Auto SELF REFRESH operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
IPP6A	**Auto Self Refresh IPP Current** Same condition with IDD6A.
IDD7	**Operating Bank Interleave Read Current** **CKE:** HIGH; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** See Table 9-1;

Symbol	Description
	BL: 8(1); **AL:** CL-1; **CS_n**: HIGH between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 9-11; **Data I/O:** Read data bursts with different data between one burst and the next one according to Table 9-11; **DM_n:** Stable at 1; **Bank Activity:** Two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 9-11; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 9-11.
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7.
IDD8	**Maximum Power Down Current** **Place DRAM in MPSM then CKE:** HIGH; **External Clock:** On; **tCK, CL:** See Table 9-1; **BL:** 8(1); **AL:** 0; **CS_n:** stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** VDDQ; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
IPP8	**Maximum Power Down IPP Current** Same condition with IDD8.

Note:

1. Burst length: BL8 fixed by MRS: set MR0[A1:0 = 00].
2. Output buffer enable:

   Set MR1 [A12=0]: Qoff=Output buffer enabled

   Set MR1 [A2:1=00]: Output Driver Impedance Control=RZQ/7

   RTT_NOM enable:

   Set MR1 [A10:8=011]: RTT_NOM=RZQ/6

   RTT_WR enable:

   Set MR2 [A10:9=01]: RTT_WR=RZQ/2

   RTT_PARK diabale:

   Set MR5 [A8:6=000]
3. CAL enabled: Set MR4 [A8:6=001]: 1600MT/s

   Set MR4 [A8:6=010]: 1866MT/s, 2133MT/s

   Set MR4 [A8:6=011]: 2400MT/s

   Gear Down mode enabled: Set MR3 [A3=1]: 1/4 Rate

   DLL disabled: Set: MR1 [A0=0]

   CA parity enabled: Set MR5 [A2:0=001]: 1600MT/s, 1866MT/s, 2133MT/s

   Set MR5 [A2:0=010]: 2400MT/s

   Read DBI enabled: Set MR5 [A12=1]

   Write DBI enabled: Set: MR5 [A11=1]

4. Low Power Auto Self Refresh (LP ASR): Set MR2 [A7:6=00]: Normal
   Set MR2 [A7:6=01]: Reduced Temperature range
   Set MR2 [A7:6=10]: Extended Temperature range
   Set MR2 [A7:6=11]: Auto Self Refresh
5. IDD2NG should be measured after sync pulse (NOP) input.

9.1.1 IDD0, IDD0A and IPP0 Measurement-Loop Pattern

Table 9-3. IDD0, IDD0A and IPP0 Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			...	Repeat pattern 1…4 until nRAS-1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern 1…4 until nRC-1, truncate if necessary																
		1	1*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=1 instead																
		2	2*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 instead																
		3	3*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=3 instead																
		4	4*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead																
		5	5*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=2 instead																
		6	6*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead																
		7	7*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=0 instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

9.1.2 IDD1, IDD1A and IPP1 Measurement-Loop Pattern

Table 9-4. IDD1, IDD1A and IPP1 Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			...	Repeat pattern 1…4 until nRCD–AL-1, truncate if necessary																
			nRCD–AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF, D2=FF, D3=00, D4=FF, D5=00, D6=00, D7=FF
			…	Repeat pattern 1…4 until nRAS-1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern 1…4 until nRC-1, truncate if necessary																
		1	1*nRC+0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC+1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC+3,4	D_#, D_#	1	1	1	1	1	0	0	3b	3	0	0	0	7	F	0	-
			…	Repeat pattern nRC+1…4 until 1*nRC+nRAS-1, truncate if necessary																
			1*nRC+nRCD–AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00, D2=00, D3=FF, D4=00, D5=FF, D6=FF, D7=00
			…	Repeat pattern 1…4 until nRAS-1, truncate if necessary																
			1*nRC+nRAS	PRE	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	-
			…	Repeat nRC+1…4 unit 2*nRC-1, truncate if necessary																
		2	2*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 instead																
		3	3*nRC	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=3 instead																
		4	4*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead																
		5	5*nRC	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=2 instead																
		6	6*nRC	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead																
		8	7*nRC	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=0 instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are VDDQ.

9.1.3 IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern

Table 9-5. IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	0
		1	4-7	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=1 instead															
		2	8-11	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 nstead															
		3	12-15	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=3 instead															
		4	16-19	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead															
		5	20-23	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=2 instead															
		6	24-27	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead															
		7	28-31	Repeat Sub-Loop 0, use BG[1:0](2)=1, BA[1:0]=0 instead															

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

9.1.4 IDD2NT and IDDQ2NT Measurement-Loop Pattern

Table 9-6. IDD2NT and IDDQ2NT Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
		1	4-7	Repeat Sub-Loop 0, but ODT=1 and BG[1:0](2)=1, BA[1:0]=1 instead															
		2	8-11	Repeat Sub-Loop 0, but ODT=0 and BG[1:0](2)=0, BA[1:0]=2 instead															
		3	12-15	Repeat Sub-Loop 0, but ODT=1 and BG[1:0](2)=1, BA[1:0]=3 instead															
		4	16-19	Repeat Sub-Loop 0, but ODT=0 and BG[1:0](2)=0, BA[1:0]=1 instead															
		5	20-23	Repeat Sub-Loop 0, but ODT=1 and BG[1:0](2)=1, BA[1:0]=2 instead															
		6	24-27	Repeat Sub-Loop 0, but ODT=0 and BG[1:0](2)=0, BA[1:0]=3 instead															
		7	28-31	Repeat Sub-Loop 0, but ODT=1 and BG[1:0](2)=1, BA[1:0]=0 instead															

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

9.1.5 IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

Table 9-7. IDD4R, IDDR4RA, IDDR4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, use BG[1:0][2]=0, BA[1:0]=2 instead															
		3	12-15	Repeat Sub-Loop 1, use BG[1:0][2]=1, BA[1:0]=3 instead															
		4	16-19	Repeat Sub-Loop 0, use BG[1:0][2]=0, BA[1:0]=1 instead															
		5	20-23	Repeat Sub-Loop 1, use BG[1:0][2]=1, BA[1:0]=2 instead															
		6	24-27	Repeat Sub-Loop 0, use BG[1:0][2]=0, BA[1:0]=3 instead															
		7	28-31	Repeat Sub-Loop 1, use BG[1:0][2]=1, BA[1:0]=0 instead															

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command.

9.1.6 IDD4W, IDDR4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern

Table 9-8. IDD4W, IDDR4WA, IDDR4WB and IDD4W_par Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 instead															
		3	12-15	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=3 instead															
		4	16-19	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead															
		5	20-23	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=2 instead															
		6	24-27	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead															
		7	28-31	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=0 instead															

Note:

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by WRITE Command.

9.1.7 IDD4WC Measurement-Loop Pattern

Table 9-9. IDD4WC Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
			5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		2	10-14	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 instead																
		3	15-19	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=3 instead																
		4	20-24	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead																
		5	25-29	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=2 instead																
		6	30-34	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead																
		7	35-39	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=0 instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by WRITE Command.

9.1.8 IDD5B Measurement-Loop Pattern

Table 9-10. IDD5B Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			4-7	Repeat pattern 1…4, use BG[1:0](2)=1, BA[1:0]=1 instead.																
			8-11	Repeat pattern 1…4, use BG[1:0](2)=0, BA[1:0]=2 instead.																
			12-15	Repeat pattern 1…4, use BG[1:0](2)=1, BA[1:0]=3 instead.																
			16-19	Repeat pattern 1…4, use BG[1:0](2)=0, BA[1:0]=1 instead.																
			20-23	Repeat pattern 1…4, use BG[1:0](2)=1, BA[1:0]=2 instead.																
			24-27	Repeat pattern 1…4, use BG[1:0](2)=0, BA[1:0]=3 instead.																
			28-31	Repeat pattern 1…4, use BG[1:0](2)=1, BA[1:0]=0 instead.																
		2	32… nRFC-1	Repeat Sub-Loop 1, Truncate, if necessary																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

9.1.9 IDD7 Measurement-Loop Pattern

Table 9-11. IDD7 Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RD A	0	1	1	0	1	0		0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			…	Repeat pattern 2…3, until nRRD-1, if nRRD>4. Truncate if necessary.																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RD A	0	1	1	0	1	0		1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	Repeat pattern 2…3, until 2*nRRD-1, if nRRD>4. Truncate if necessary.																
		2	2*nRRD	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=2 instead.																
		3	3*nRRD	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=3 instead.																
		4	4*nRRD	Repeat pattern 2…3, until nFAW-1, if nFAW>4*nRRD. Truncate if necessary.																
		5	nFAW	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=1 instead.																
		6	nFAW+nRRD	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=2 instead.																
		7	nFAW+2*nRRD	Repeat Sub-Loop 0, use BG[1:0](2)=0, BA[1:0]=3 instead.																
		8	nFAW+3*nRRD	Repeat Sub-Loop 1, use BG[1:0](2)=1, BA[1:0]=0 instead.																
		9	nFAW+4*nRRD	Repeat Sub-Loop 4																
		10	2*nFAW	repeat pattern 2…3, until nRC-1, if nRC->-2-*-nFAW. Truncate if necessary.																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are VDDQ.

9.2 IDD Specifications

IDD and IPP values are for full operation range of voltage and temperature unless otherwise noted.

Table 9-12. IDD and IDDQ Specifications

Symbol	Width	2400	2666	3200	Unit
IDD0	x16	83	86	91	mA
IDD1	x16	105	108	115	mA
IDD2N	x16	65	68	74	mA
IDD2NT	x16	74	78	85	mA
IDD2P	x16	47	47	48	mA
IDD2Q	x16	62	65	70	mA
IDD3N	x16	93	96	101	mA
IDD3P	x16	69	69	71	mA
IDD4R	x16	216	232	263	mA
IDD4W	x16	200	215	243	mA
IDD5R	x16	76	80	85	mA
IDD6N	x16	65	65	65	mA
IDD6E	x16	78	78	78	mA
IDD6R	x16	64	64	64	mA
IDD6A	x16	78	78	78	mA
IDD7	x16	266	272	282	mA

Table 9-13. IPP Specifications

Symbol	Width	2400	2666	3200	Unit
IPP0	x16	6	6	6	mA
IPP3N	x16	10	10	10	mA
IPP5R	x16	5	5	5	mA
IPP7	x16	25	25	25	mA

Table 9-14. IDD6 Specification

Symbol	Temperature Range	Width	2400	2666	3200	Unit	Note
IDD6N	0°C~85°C	x16	65	65	65	mA	3,4
IDD6E	0°C~95°C	x16	78	78	78	mA	4,5,6
IDD6R	0°C~45°C	x16	64	64	64	mA	4,6,9
IDD6A	0°C~95°C	x16	78	78	78	mA	4,6,7,8

Note:

1. Some IDD currents are higher for x16 organization due to larger page size architecture.
2. Max values for IDD currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6=0 and A7=0.
4. Datasheet include a max value for IDD6.
5. Applicable for MR2 settings A6=0 and A7=1. IDD6E is only specified for devices which support the Extended Temperature Range feature.
6. Refer to datasheet for the value specification method (e.g. max, typical) for IDD6E and IDD6A.
7. Applicable for MR2 settings A6=1 and A7=0. IDD6A is only specified for devices which support the Auto Self Refresh feature.

8. The number of discrete temperature ranges supported and the associated Ta-Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data shee t for more information.
9. Applicable for MR2 settings MR2 [A7:A6=01]: Reduced Temperature range. IDD6R is verified by design and characterization, and may not be subject to production test.

10 Input/Output Capacitance

Table 10-1. Silicon Pad I/O Capacitance

Parameter	Symbol	1600/1866/2133		2400/2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
Input/output capacitance	C_{IO}	0.55	1.4	0.55	1.15	0.55	1.00	pF	1,2,3
Input/output capacitance delta	C_{DIO}	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
Input/output capacitance delta DQS_t and DQS_c	C_{DDQS}	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
Input capacitance, CK_t and CK_c	C_{CK}	0.2	0.8	0.2	0.7	0.2	0.7	pF	1,3
Input capacitance delta CK_t and CK_c	C_{DCK}	-	0.05	-	0.05	-	0.05	pF	1,3,4
Input capacitance (CTRL, ADD, CMD pins only)	C_I	0.2	0.8	0.2	0.7	0.2	0.55	pF	1,3,6
Input capacitance delta (All CTRL pins only)	C_{DI_CTRL}	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
Input capacitance delta (All ADD/CMD pins only)	$C_{DI\_ADD\_CMD}$	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
Input/output capacitance of ALERT	C_{ALERT}	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
Input/output capacitance of ZQ	C_{ZQ}	-	2.3	-	2.3	-	2.3	pF	1,3,12
Input capacitance of TEN	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by deembedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating.
2. DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c. Although the DM, TDQS_t and TDQS_c pins have different functions, the loading matches DQ and DQS.
3. This parameter applies to monolithic devices only; stacked/dual die devices are not covered here.
4. Absolute value of CK_t-CK_c.
5. Absolute value of C_{IO}(DQS_t)-C_{IO}(DQS_c).
6. CI applies to ODT, CS_n, CKE, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. C_{DI_CTRL} applies to ODT, CS_n and CKE.
8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CK_t)+C_I(CK_c)).
9. $C_{DI\_ADD\_CMD}$ applies to, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD)-0.5*(C_I(CK_t)+C_I(CK_c)).

11. $C_{DIO}=C_{IO}(DQ, DM)-0.5*(C_{IO}(DQS\_t)+C_{IO}(DQS\_c))$.
12. Maximum external load capacitance on ZQ pin: 5pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

Table 10-2. DRAM Package Electrical Specifications (x16)

Parameter		Symbol	1600/1866/2133/ 2400/2666		2933		3200		Unit	Note
			Min	Max	Min	Max	Min	Max		
Input/output	Zpkg	Z_{IO}	45	85	45	85	45	85	Ω	1, 2, 4
	Package delay	Td_{IO}	14	45	14	45	14	45	ps	1, 3, 4
	Lpkg	L_{io}	—	3.4	—	3.4	—	3.4	nH	11
	Cpkg	C_{io}	—	0.82	—	0.82	—	0.82	pF	11
LDQS_t/LDQS_c/ UDQS_t/UDQS_c	Zpkg	$Z_{IO\ DQS}$	45	85	45	85	45	85	Ω	1, 2
	Package delay	$Td_{IO\ DQS}$	14	45	14	45	14	45	ps	1, 3
	Lpkg	$L_{io\ DQS}$	—	3.4	—	3.4	—	3.4	nH	11
	Cpkg	$C_{io\ DQS}$	—	0.82	—	0.82	—	0.82	pF	11
LDQS_t/ LDQS_c/ UDQS_t/UDQS_c	Delta Zpkg	$DZ_{DIO\ DQS}$	—	10.5	—	10.5	—	10.5	Ω	1, 2, 6
	Delta delay	$DTd_{DIO\ DQS}$	—	5	—	5	—	5	ps	1, 3, 6
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	50	90	50	90	50	90	Ω	1, 2, 8
	Package delay	$Td_{I\ CTRL}$	14	42	14	42	14	42	ps	1, 3, 8
	Lpkg	$L_{i\ CTRL}$	—	3.4	—	3.4	—	3.4	nH	11
	Cpkg	$C_{i\ CTRL}$	—	0.7	—	0.7	—	0.7	pF	11
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	50	90	50	90	50	90	Ω	1, 2, 7
	Package delay	$Td_{I\ ADD\ CMD}$	14	52	14	52	14	52	ps	1, 3, 7
	Lpkg	$L_{i\ ADD\ CMD}$	—	3.9	—	3.9	—	3.9	nH	11
	Cpkg	$C_{i\ ADD\ CMD}$	—	0.86	—	0.86	—	0.86	pF	11
CK_t, CK_c	Zpkg	Z_{CK}	50	90	50	90	50	90	Ω	1, 2
	Package delay	Td_{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ_{DCK}	—	10.5	—	10.5	—	10.5	Ω	1, 2, 5

Parameter		Symbol	1600/1866/2133/ 2400/2666		2933		3200		Unit	Note
			Min	Max	Min	Max	Min	Max		
	Delta delay	DTd_{DCK}	—	5	—	5	—	5	ps	1, 3, 5
Input CLK	Lpkg	$L_{i\ CLK}$	—	3.4	—	3.4	—	3.4	nH	11
	Cpkg	$C_{i\ CLK}$	—	0.7	—	0.7	—	0.7	pF	11
ZQ Zpkg		$Z_{O\ ZQ}$	—	100	—	100	—	100	Ω	1, 2
ZQ delay		$Td_{O\ ZQ}$	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		$Z_{O\ ALERT}$	40	100	40	100	40	100	Ω	1, 2
ALERT delay		$Td_{O\ ALERT}$	20	55	20	55	20	55	ps	1, 3

Note:

1. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS, and VSSQ shorted and all other signal pins shorted at the die, not pin, side.
2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin)=SQRT(Lpkg/Cpkg).
3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin)=SQRT(Lpkg*Cpkg).
4. Z_{IO} and Td_{IO} apply to DQ, DM, TDQS_t and TDQS_c.
5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
6. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
7. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.
8. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
10. It is assumed that Lpkg can be approximated as $Lpkg=Z_O*Td$.
11. It is assumed that Cpkg can be approximated as $Cpkg=Td/Z_O$.

11 Electrical Characteristics and AC Timing

11.1 Reference Load for AC Timing and Output Slew Rate

Figure 11-1 represents the effective reference load of 50Ω used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34Ω to specify the relevant AC timing parameter values of the device.

- The maximum DC high level of output signal=1.0*VDDQ
- The minimum DC low level of output signal={34/(34+50)}*VDDQ=0.4*VDDQ
- The nominal reference level of an output signal can be approximated by the following:
- The center of maximum DC high and minimum DC low={(1+0.4)/2}*VDDQ=0.7*VDDQ

The actual reference level of output signal might vary with driver RON and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

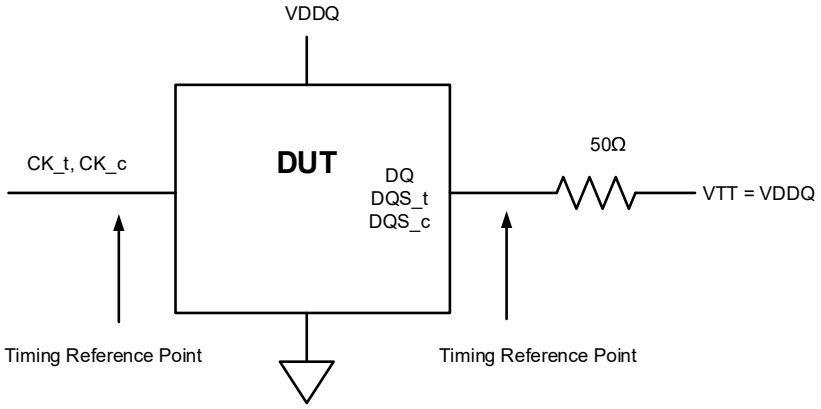


Figure 11-1. Reference Load for AC Timing and Output Slew Rate

11.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in Table 11-1 below.

Table 11-1. tREFI by Device Density

Parameter	Symbol		4Gb	Unit
Average periodic refresh interval	tREFI	-40°C≤T_{CASE}≤85°C	7.8	us
		85°C<T_{CASE}≤95°C	3.9	us

11.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

11.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

11.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle windows, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg)=(\sum_{j=1}^{N} tCK(abs)_j)/N \quad N=200$$

11.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg)=(\sum_{j=1}^{N} tCH_j)/(N*tCK(avg)) \quad N=200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg)=(\sum_{j=1}^{N} tCL_j)/(N*tCK(avg)) \quad N=200$$

11.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n*tCK(avg). tERR is not subject to production test.

11.4 Timing Parameters by Speed Grade

11.4.1 Timing Parameters by Speed Bin for DDR4-1600 to 2400

Table 11-2. Timing Parameters by Speed Bin for DDR4-1600 to 2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	20	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	ns	34,35
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	-
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	-
Absolute Clock Period	tCK(abs)	Min: tCK(avg)min+tJIT(per)min_tot								tCK(avg)	-
		Max: tCK(avg)max+tJIT(per)max_tot									
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	tJIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	tJIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	-
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	ps	-
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	ps	-
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	-
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps	-
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	-
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	-
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	-
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	-
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	-
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	-
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps	-
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	-
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps	-
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps	-
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps	-
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	ps	-
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps	-
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps	-
Cumulative error across n=13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min=((1+0.68ln(n))*tJIT(per)_total min) tERR(nper)max=((1+0.68ln(n))*tJIT(per)_total max)								ps	-
Command and Address setup time to CK_t, CK_c referenced to VIH(AC)/VIL(AC) levels	tIS(base)	115	-	100	-	80	-	62	-	ps	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Command and Address setup time to CK_t, CK_c referenced to VREF levels	tIS(VREF)	215	-	200	-	180	-	162	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to VIH(DC)/VIL(DC) levels	tIH(base)	140	-	125	-	105	-	87	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to VREF levels	tIH(VREF)	215	-	200	-	180	-	162	-	ps	-
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	-
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max (5nCK, 6.250ns)	-	Max (5nCK, 5.355ns)	-	Max (5nCK, 5.355ns)	-	Max (5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max (4nCK, 6ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max (4nCK, 5ns)	-	Max (4nCK, 4.2ns)	-	Max (4nCK, 3.7ns)	-	Max (4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max (4nCK, 5.0ns)	-	Max (4nCK, 4.2ns)	-	Max (4nCK, 3.7ns)	-	Max (4nCK, 3.3ns)	-	nCK	34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max (4nCK, 7.5ns)	-	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max (4nCK, 6.0ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max (4nCK, 6.0ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW(2K)	Max (28nCK, 35ns)	-	Max (28nCK, 30ns)	-	Max (28nCK, 30ns)	-	Max (28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW(1K)	Max (20nCK, 25ns)	-	Max (20nCK, 23ns)	-	Max (20nCK, 21ns)	-	Max (20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW(1/2K)	Max (16nCK, 20ns)	-	Max (16nCK, 17ns)	-	Max (16nCK, 15ns)	-	Max (16nCK, 13ns)	-	ns	34
Delay from start of internal WRITE transaction to internal READ command for different bank group	tWTR_S	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	ns	1,34
Delay from start of internal WRITE transaction to internal READ command for same bank group	tWTR_L	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	1,34
Internal READ command to PRECHARGE command delay	tRTP	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	-
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+Max (4nCK, 3.75ns)	-	tWR+Max (5nCK, 3.75ns)	-	tWR+Max (5nCK, 3.75ns)	-	tWR+Max (5nCK, 3.75ns)	-	ns	1,28

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Delay from start of internal WRITE transaction to internal READ command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+Max (4nCK, 3.75ns)	-	tWTR_S+Max (5nCK, 3.75ns)	-	tWTR_S+Max (5nCK, 3.75ns)	-	tWTR_S+Max (5nCK, 3.75ns)	-	ns	2,29
Delay from start of internal WRITE transaction to internal READ command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+Max (4nCK, 3.75ns)	-	tWTR_L+Max (5nCK, 3.75ns)	-	tWTR_L+Max (5nCK, 3.75ns)	-	tWTR_L+Max (5nCK, 3.75ns)	-	ns	2,30
DDL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	-
MODE REGISTER SET command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	-
MODE REGISTER SET command update delay	tMOD	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	nCK	50
Mult-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	tWR_MPR	tMODmin+AL+PL	-	tMODmin+AL+PL	-	tMODmin+AL+PL	-	tMODmin+AL+PL	-	ns	-
Auto precharge write recovery + precharge time	tDALmin	Programmed WR+roundup (tRP/tCK(avg))								nCK	-
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,46
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,46
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	nCK	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
MODE REGISTER SET command cycle time in CAL mode	tMRD_CAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	-
MODE REGISTER SET update delay in CAL mode	tMOD_CAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	-
DRAM Data Timing											
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	tCK(avg)/2	13,17,38
DQ output hold time per group, pre access from DQS_t, DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK(avg)/2	13,16,17,38
Data Valid Window per device per UI: (tQH-tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	16,17,38
Data Valid Window per pin per UI: (tQH-tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	16,17,38
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	-330	175	ps	38
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	ps	38
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note44	0.9	Note44	0.9	Note44	0.9	Note44	nCK	39,40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	N/A	N/A	NA	N/A	N/A	N/A	1.8	Note44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note45	0.33	Note45	0.33	Note45	0.33	Note45	tCK	39

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA	NA	NA	NA	NA	NA	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	-
DQS_t and DQS_c low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	-
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	-
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	N/A	N/A	N/A	N/A	N/A	N/A	-0.5	0.5	-	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	-
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	-
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	370	-	330	-	310	-	290	ps	36,37,38
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DLL on mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	ps	36,37,38
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tCK	-
Valid clock requirement after MPSM entry	tCKMPE	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tMODmin+tCPDEDmin	-	tCK	-
Valid clock requirement before MPSM exit	tCKMPX	tCKSRXmin	-	tCKSRXmin	-	tCKSRXmin	-	tCKSRXmin	-	tCK	-
Exit MPSM to commands not requiring a locked DLL	tXMP	tXSmin	-	tXSmin	-	tXSmin	-	tXSmin	-	tCK	-
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMPmin+tXSDLLmin	-	tXMPmin+tXSDLLmin	-	tXMPmin+tXSDLLmin	-	tXMPmin+tXSDLLmin	-	tCK	-
CS setup time to CKE	tMPX_S	tISmin+tIHmin	-	tISmin+tIHmin	-	tISmin+tIHmin	-	tISmin+tIHmin	-	ns	-
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	-
Normal operation short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	-
Reset/Self Refresh Timing											
Exit reset from CKE HIGH to a valid command	tXPR	Max (5nCK, tRFCmin+10ns)	-	Max (5nCK, tRFCmin+10ns)	-	Max (5nCK, tRFCmin+10ns)	-	Max (5nCK, tRFCmin+10ns)	-	nCK	-
Exit self refresh to commands not requiring a locked DLL	tXS	tRFCmin+10ns	-	tRFCmin+10ns	-	tRFCmin+10ns	-	tRFCmin+10ns	-	nCK	-
SRX to Commands not requiring a locked DLL in self refresh abort	tXS_ABORTmin	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	nCK	-
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FASTmin	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	nCK	-
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLLKmin	-	tDLLKmin	-	tDLLKmin	-	tDLLKmin	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing	tCKESR	tCKEmin+1nCK	-	tCKEmin+1nCK	-	tCKEmin+1nCK	-	tCKEmin+1nCK	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKEmin+1nCK+PL	-	tCKEmin+1nCK+PL	-	tCKEmin+1nCK+PL	-	tCKEmin+1nCK+PL	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	nCK	-
Valid Clock Requirement before self refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Power Down Timing											
Exit power-down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	nCK	-
CKE minimum pulse width	tCKE	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	-
Power Down Entry to Exit Timing	tPD	tCKEmin	9 * tREFI	tCKEmin	9 * tREFI	tCKEmin	9 * tREFI	tCKEmin	9 * tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	nCK	4

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+ (tWR/tCK(avg))	-	WL+2 + (tWR/tCK(avg))	-	WL+2 + (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMODmin	-	tMODmin	-	tMODmin	-	tMODmin	-	nCK	-
PDA Timing											
MODE REGISTER SET command cycle time in PDA mode	tMRD_PDA	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	-
MODE REGISTER SET command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	-
ODT Timing											
Asynchronous R_{TT} turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	1	9	1	9	1	9	ns	-
Asynchronous R_{TT} turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	1	9	1	9	ns	-
R_{TT} dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	-
Write Leveling Timing											
First DQS_t/DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	-
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	-
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	-
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	-
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	-
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	-
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	-
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	-
Parity Latency	PL	4		4		4		5		nCK	-
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CRC ALERT_n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	-
tREFI											
tRFC1min	4Gb	260	-	260	-	260	-	260	-	ns	34
tRFC2min	4Gb	160	-	160	-	160	-	160	-	ns	34
tRFC4min	4Gb	110	-	110	-	110	-	110	-	ns	34

11.4.2 Timing Parameters by Speed Bin for DDR4-2666 to 3200

Table 11-3. Timing Parameters by Speed Bin for DDR4-2666 to 3200

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	0.75	<0.833	0.682	<0.750	0.625	<0.682	ns	34,35
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	-
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	-
Absolute Clock Period	tCK(abs)	Min=tCK(avg)min+tJIT(per)min_tot						tCK(avg)	-
		Max=tCK(avg)max+tJIT(per)max_tot							
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter-total	tJIT(per)_tot	-38	38	-34	34	-32	32	ps	25
Clock Period Jitter-deterministic	tJIT(per)_dj	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	-27	27	-25	25	ps	-
Cycle to Cycle Period Jitter	tJIT(cc)	-	75	-	68	-	62	ps	25
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	60	-	55	-	50	ps	-
Cumulative error across 2 cycles	tERR(2per)	-55	55	-50	50	-46	46	ps	-
Cumulative error across 3 cycles	tERR(3per)	-66	66	-60	60	-55	55	ps	-
Cumulative error across 4 cycles	tERR(4per)	-73	73	-66	66	-61	61	ps	-
Cumulative error across 5 cycles	tERR(5per)	-78	78	-71	71	-65	65	ps	-
Cumulative error across 6 cycles	tERR(6per)	-83	83	-75	75	-69	69	ps	-
Cumulative error across 7 cycles	tERR(7per)	-87	87	-79	79	-73	73	ps	-
Cumulative error across 8 cycles	tERR(8per)	-91	91	-83	83	-76	76	ps	-
Cumulative error across 9 cycles	tERR(9per)	-94	94	-85	85	-78	78	ps	-
Cumulative error across 10 cycles	tERR(10per)	-96	96	-88	88	-80	80	ps	-
Cumulative error across 11 cycles	tERR(11per)	-99	99	-90	90	-83	83	ps	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Cumulative error across 12 cycles	tERR(12per)	-101	101	-92	92	-84	84	ps	-
Cumulative error across 13 cycles	tERR(13per)	-103	103	-93	93	-86	86	ps	-
Cumulative error across 14 cycles	tERR(14per)	-104	104	-95	95	-87	87	ps	-
Cumulative error across 15 cycles	tERR(15per)	-106	106	-97	97	-89	89	ps	-
Cumulative error across 16 cycles	tERR(16per)	-108	108	-98	98	-90	90	ps	-
Cumulative error across 17 cycles	tERR(17per)	-110	110	-100	100	-92	92	ps	-
Cumulative error across 18 cycles	tERR(18per)	-112	112	-101	101	-93	93	ps	-
Cumulative error across n=13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min=((1+0.68ln(n))*tJIT(per)_totalmin)						ps	-
		tERR(nper)max=((1+0.68ln(n))*tJIT(per)_totalmax)							
Command and Address setup time to CK_t, CK_c referenced to VIH(AC)/VIL(AC) levels	tIS(base)	55	-	48	-	40	-	ps	-
Command and Address setup time to CK_t, CK_c referenced to VREF levels	tIS(VREF)	145	-	138	-	130	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to VIH(DC)/VIL(DC) levels	tIH(base)	80	-	73	-	65	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to VREF levels	tIH(VREF)	145	-	138	-	130	-	ps	-
Control and Address Input pulse width for each input	tIPW	385	-	365	-	340	-	ps	-
Command and Address Timing-									
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5ns)	-	Max(5nCK, 5ns)	-	Max(5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	Max(4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Four activate window for 2KB page size	tFAW(2K)	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW(1K)	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW(1/2K)	Max(16nCK, 12ns)	-	Max(16nCK, 10.875ns)	-	Max(16nCK, 10ns)	-	ns	34
Delay from start of internal WRITE transaction to internal READ command for different bank group	tWTR_S	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	Max(2nCK, 2.5ns)	-	ns	1,34
Delay from start of internal WRITE transaction to internal READ command for same bank group	tWTR_L	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRCHARGE command delay	tRTP	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-	ns	-
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+Max(5nCK, 3.75ns)	-	tWR+Max(5nCK, 3.75ns)	-	tWR+Max(5nCK, 3.75ns)	-	ns	1,28
Delay from start of internal WRITE transaction to internal READ command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+Max(5nCK, 3.75ns)	-	tWTR_S+Max(5nCK, 3.75ns)	-	tWTR_S+Max(5nCK, 3.75ns)	-	ns	2,29
Delay from start of internal WRITE transaction to internal READ command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+Max(5nCK, 3.75ns)	-	tWTR_L+Max(5nCK, 3.75ns)	-	tWTR_L+Max(5nCK, 3.75ns)	-	ns	2,30
DDL locking time	tDLLK	1024	-	1024	-	1024	-	nCK	-
MODE REGISTER SET command cycle time	tMRD	8	-	8	-	8	-	nCK	-
MODE REGISTER SET command update delay	tMOD	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	Max(24nCK, 15ns)	-	nCK	-
Mult-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	tWR_MPR	tMODmin+AL+PL	-	tMODmin+AL+PL	-	tMODmin+AL+PL	-	nCK	-
Auto precharge write recovery + precharge time	tDALmin	Programmed WR+roundup (tRP/tCK(avg))						nCK	-
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,46
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	45,46
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	nCK	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
MODE REGISTER SET command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	-
MODE REGISTER SET update delay in CAL mode	tMOD_tCAL	tMOD+tCAL	-	tMOD+tCAL	-	tMOD+tCAL	-	nCK	-
DRAM Data Timing									
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	-	0.19	-	0.20	tCK(avg)/2	13,17,38
DQ output hold time per group, per access from QDS_t, DQS_c	tQH	0.74	-	0.72	-	0.70	-	tCK(avg)/2	13,16,17,38
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	0.64	-	0.64	-	UI	-
Data Valid Window per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.72	-	0.72	-	UI	-
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-310	170	-280	165	-250	160	ps	-
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	170	-	165	-	160	ps	-
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	tRPRE	0.9	Note44	0.9	Note44	0.9	Note44	tCK	-
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	1.8	Note44	1.8	Note44	1.8	Note44	tCK	-
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note45	0.33	Note45	0.33	Note45	tCK	-
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	-
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	-	165	-	160	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	-
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	TBD	TBD	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	-
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	-
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	270	-	265	-	260	ps	36,37,38
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DDL on mode	tDQSCK(DLL On)	-170	170	-165	165	-160	160	ps	36,37,38
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMODmin+ tCPDEDmin	-	tMODmin+ tCPDEDmin	-	tMODmin+ tCPDEDmin	-	tCK	-
Valid clock requirement after MPSM entry	tCKMPE	tMODmin+ tCPDEDmin	-	tMODmin+ tCPDEDmin	-	tMODmin+ tCPDEDmin	-	tCK	-
Valid clock requirement before MPSM exit	tCKMPX	tCKSRXmin	-	tCKSRXmin	-	tCKSRXmin	-	tCK	-
Exit MPSM to commands not requiring a locked DLL	tXMP	tXSmin	-	tXSmin	-	tXSmin	-	tCK	-
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMPmin+ tXSDLLmin	-	tXMPmin+ tXSDLLmin	-	tXMPmin+ tXSDLLmin	-	tCK	-
CS setup time to CKE	tMPX_S	tISmin+tIHmin	-	tISmin+tIHmin	-	tISmin+tIHmin	-	ns	-
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	-
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	-
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	-
Reset/Self Refresh Timing									
Exit reset from CKE HIGH to a valid command	tXPR	Max(5nCK, tRFCmin+10ns)	-	Max(5nCK, tRFCmin+10ns)	-	Max(5nCK, tRFCmin+10ns)	-	nCK	-
Exit self refresh to commands not requiring a locked DLL	tXS	tRFCmin+10ns	-	tRFCmin+10ns	-	tRFCmin+10ns	-	nCK	-
SRX to commands not requiring a locked DLL in self refresh abort	tXS_ABORTmin	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	nCK	-
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FASTmin	tRFC4min+10ns	-	tRFC4min+10ns	-	tRFC4min+10ns	-	nCK	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLLKmin	-	tDLLKmin	-	tDLLKmin	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing	tCKESR	tCKEmin+1nCK	-	tCKEmin+1nCK	-	tCKEmin+1nCK	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKEmin+1nCK+PL	-	tCKEmin+1nCK+PL	-	tCKEmin+1nCK+PL	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	nCK	-
Valid Clock Requirement before self refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Power Down Timing									
Exit Power Down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	Max(4nCK, 6ns)	-	nCK	-
CKE minimum pulse width	tCKE	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	Max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	-
Power Down Entry to Exit Timing	tPD	tCKEmin	9 * tREFI	tCKEmin	9 * tREFI	tCKEmin	9 * tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR/tCK(avg))	-	WL+4+ (tWR/tCK(avg))	-	WL+4 + (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	WL+2+ (tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMODmin	-	tMODmin	-	tMODmin	-	nCK	-
PDA Timing									
MODE REGISTER SET command cycle time in PDA mode	tMRD_PDA	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
MODE REGISTER SET command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		nCK	-
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	1	9	1	9	ns	-
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	1	9	ns	-
RTT dynamic change skew	tADC	0.28	0.72	0.26	0.74	0.26	0.74	tCK(avg)	-
Write Leveling Timing									
First DQS_t/DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	-
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	-
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	-
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	-
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	nCK	-
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	-
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	80	160	88	176	96	192	nCK	-
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	71	-	78	-	85	nCK	-
Parity Latency	PL	5		6		6		nCK	-
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	-
CRC ALERT_n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10	nCK	-
Gear Down Timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR	-	tXPR	-	tXPR	-	-	-

Speed		2666		2933		3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
CKE High Assert to Gear Down Enable time (T2/CKE)	tXS_GEAR	tXS	-	tXS	-	tXS	-	-	-
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD+4nCK	-	tMOD+4nCK	-	tMOD+4nCK	-	-	27
Sync pulse to First valid command(T4)	tCMD_GEAR	tMOD	-	tMOD	-	tMOD	-	-	27
Geardown setup time	tGEAR setup	2	-	2	-	2	-	nCK	-
Geardown hold time	tGEAR hold	2	-	2	-	2	-	nCK	-
tREFI									
tRFC1	4Gb	260	-	260	-	260	-	ns	34
tRFC2	4Gb	160	-	160	-	160	-	ns	34
tRFC4	4Gb	110	-	110	-	110	-	ns	34

Note:

1. Start of internal WRITE transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (Fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are READ (and Read Auto Precharge) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rouding algorithm defined in Section 11.5.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on T_{OPER}.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM [nCK]=ROUND UP{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled, tWTR_S_CRC_DM is used in place of tWTR_S.

11. When CRC and DM are both enabled, tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max value is system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing.
15. DQ to DQ static offset relative to strobe per group.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock).
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled, tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled, tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VIL(DC) for tCKE specification (low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIH(DC) for tCKE specification (high pulse width).
33. Defined between end of MPR Read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Section 8.
35. This parameter must keep consistency with Section 8.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600MT/s data rate. UI=tCK(avg)min/2.

37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RONnom=34Ω.
40. 1tCK toggle mode with setting MR4: A11 to 0.
41. 2tCK toggle mode with setting MR4: A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4: A12 to 0.
43. 2tCK mode with setting MR4: A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCKmax on the right side.
45. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS diff-signal cross-point.
46. Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from LOW to HIGH.
47. VREFDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCKmin plus tQSHmin on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7*VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 Ω and an effective test load of 50Ω to VTT=VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

11.5 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33MHz which yields a clock period of 1.0714ns. Similarly, a system with a memory clock frequency of 1066.66MHz yields mathematically a clock period of 0.9375ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCK(avg)min are defined to 1ps of accuracy; for example, 0.9375ns is defined as 937ps and 1.0714ns is defined as 1071ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:
  nCK=ceiling [(parameter_in_ns/application_tCK_ in_ns)-0.025]
- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:
  nCK=truncate [{(parameter_in_ps*1000)/(application_tCK_in_ps)+974}/1000]
- Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect (SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm:
  nCK = ceiling (parameter_in_ns/application_tCK_in_ns).

11.6 The DQ Input Receiver Compliance Mask for Voltage and Timing

The DQ input receiver compliance mask for voltage and timing is shown in Figure 11-2 below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. Any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

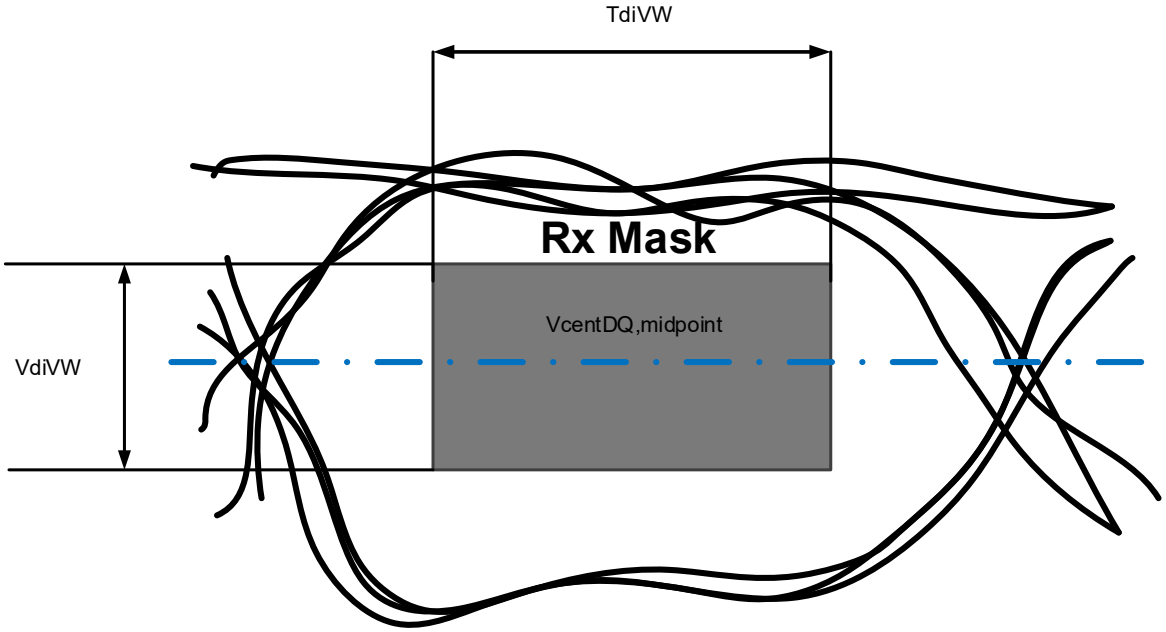


Figure 11-2. DQ Receiver (Rx) Compliance mask

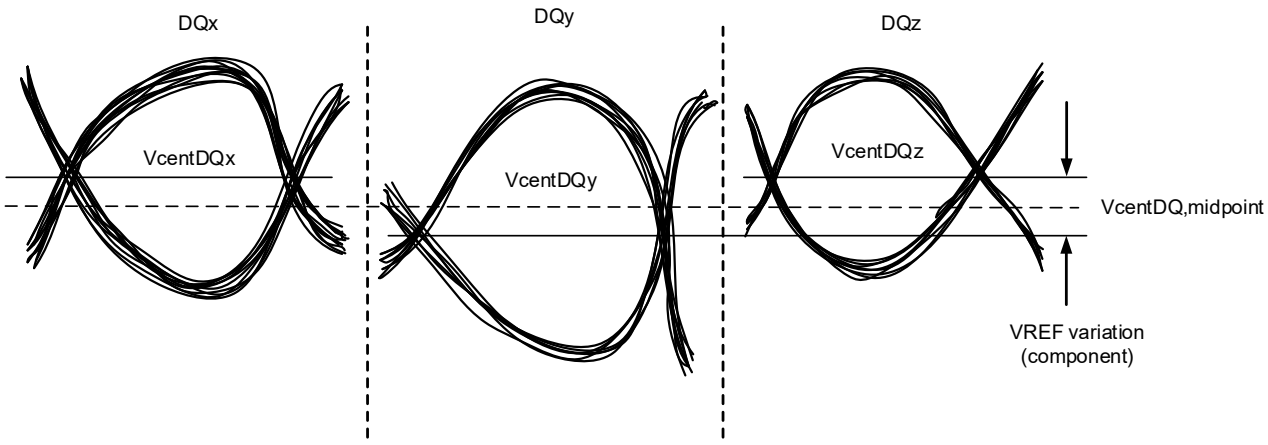


Figure 11-3. Across Pin V_{REFDQ} Voltage Variation

The VREFDQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally VcentDQ,midpoint, in order to have valid Rx Mask values.

VcentDQ,midpoint is defined as the midpoint between the largest VREFDQ voltage level and the smallest VREFDQ voltage level across all DQ pins for a given DRAM component. Each DQ pin VREF level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 11-3. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for RON and ODT settings.

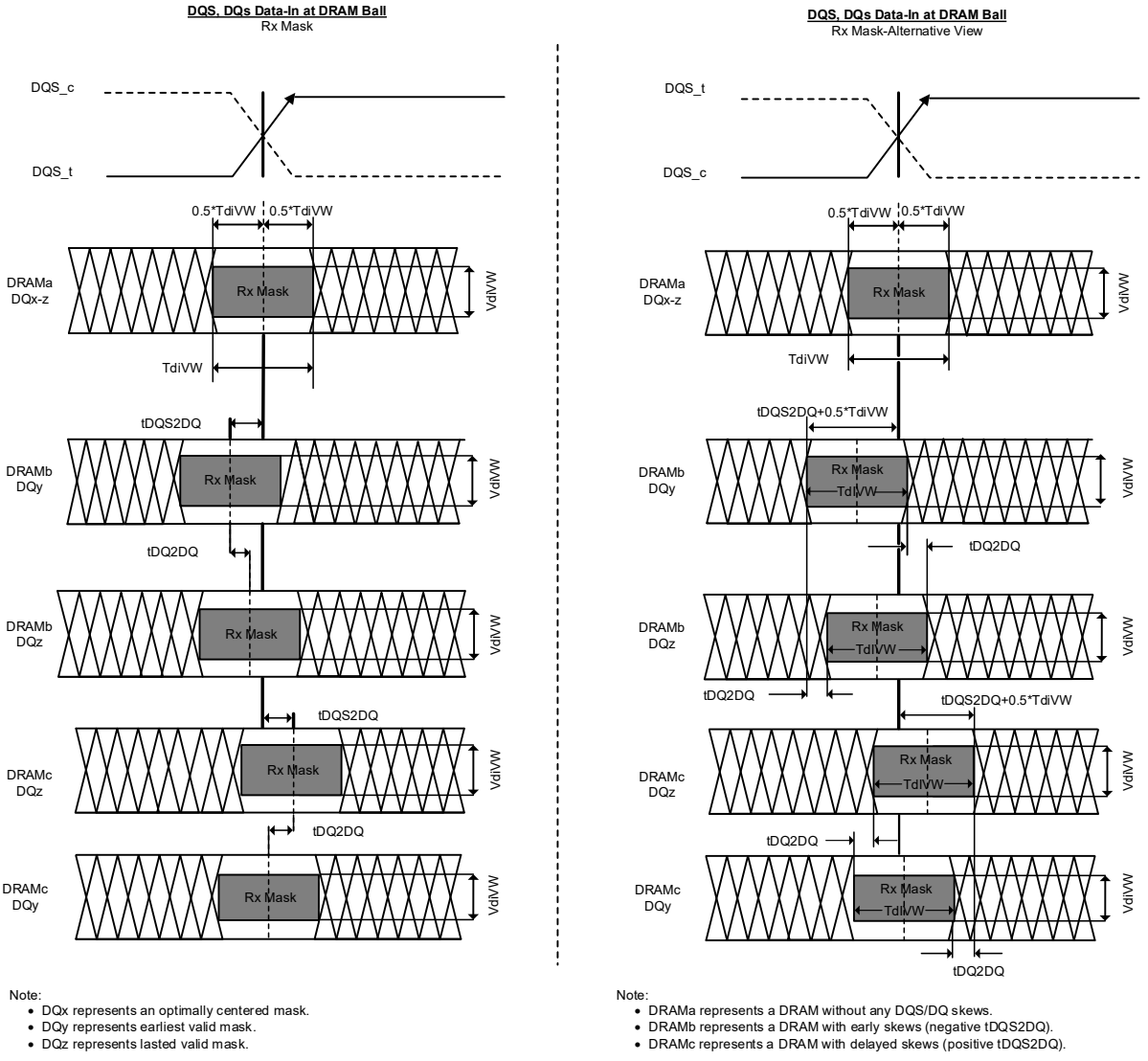


Figure 11-4. DQS to DQ and DQ to DQ Timings at DRAM Balls

Note:

1. Figures show skew allowed between DRAM to DRAM and between DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
2. TdiPW is not shown; composite data-eyes shown would violate TdiPW.
3. VcentDQ,midpoint is not shown but is assumed to be midpoint of VdiVW.

All of the timing term in Figure 11-5 are measured at the VdiVW voltage levels centered around VcentDQ,midpoint and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 11-6 below: A LOW to HIGH transition tr1 is measured from 0.5*VdiVWmax below VcentDQ,midpoint to the last transition through 0.5*VdiVWmax above VcentDQ,midpoint while tr2 is measured from the last transition through 0.5*VdiVWmax above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL(AC)min above VcentDQ,midpoint.

Rising edge slew rate equations:

- srr1=VdiVWmax/tr1
- srr2=(VIHL(AC)min–VdiVWmax)/(2*tr2)

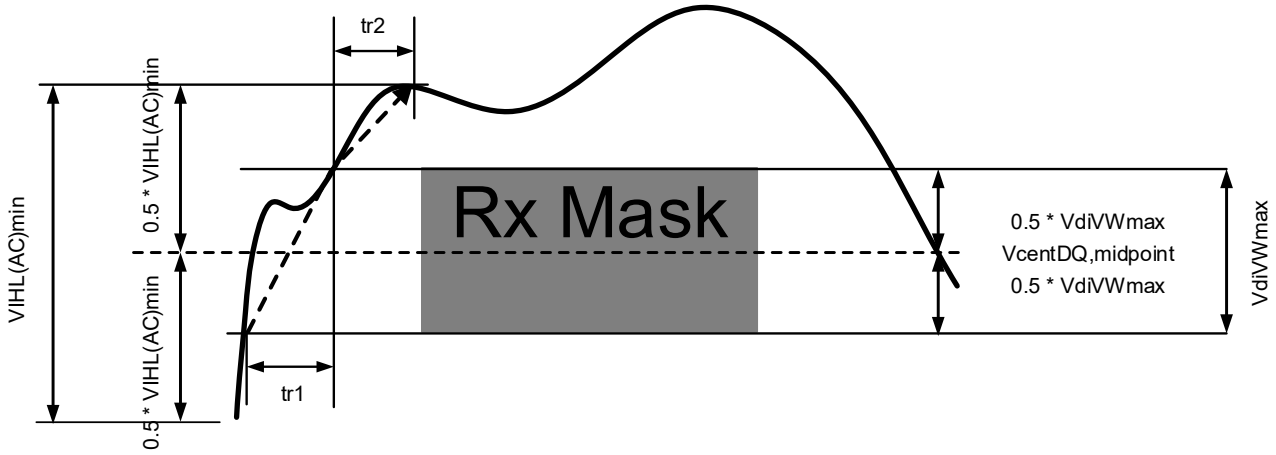


Figure 11-5. Slew Rate Conditions for Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 11-6 below: A HIGH to LOW transition tf1 is measured from 0.5*VdiVWmax above VcentDQmidpoint to the last transition through 0.5*VdiVWmax below VcentDQ,midpoint while tf2 is measured from the last transition through 0.5*VdiVWmax below VcentDQ,midpoint to the first transition through the 0.5*VIHL(AC)min below VcentDQ (pin mid).
Falling edge slew rate equations:

- srf1=VdiVWmax/tf1
- srf2=(VIHL(AC)min-VdiVWmax)/(2*tf2)

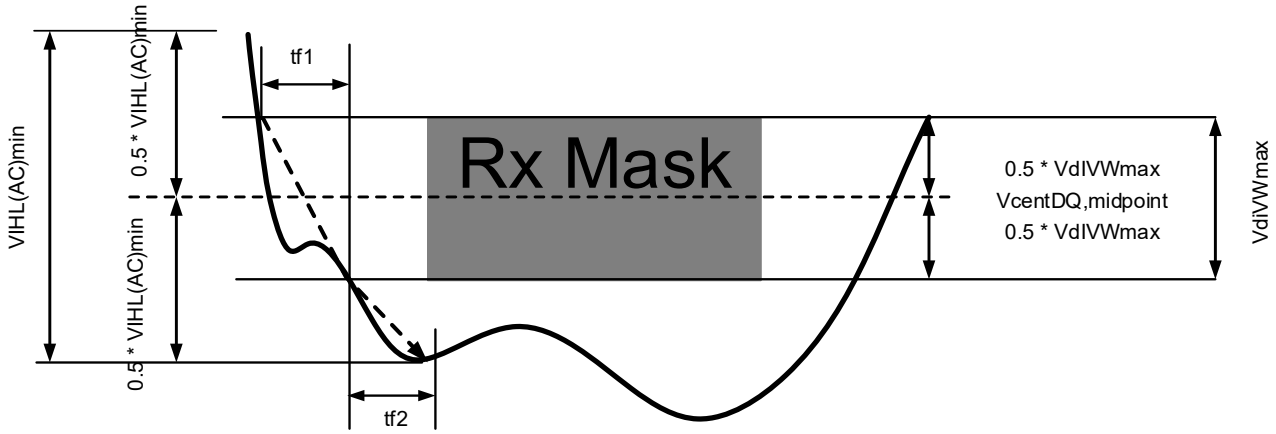


Figure 11-6. Slew Rate Conditions for Falling Transition

Table 11-4. DRAM DQs in Receive Mode; UI=tCK(avg)min/2

Symbol	Parameter	1600/1866/2133		2400		2666		2933		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VdiVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	115	-	110	mV	1,2,10
TdiVW	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	-	0.23	UI	1,2,10
VIHL(AC)	DQ AC input swing pk-pk	186	-	160	-	150	-	145	-	140	-	mV	3,4,10
TdiPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	0.58	-	UI	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI	6,10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.1	-	0.1	-	0.105	-	0.115	-	0.125	UI	7
srr1 srf1	Input Slew Rate over VdIVW if tCK≥0.937ns	1.0	9	1.0	9	1.0	9	1	9	1.0	9	V/ns	8,10
srf1 srf2	Input Slew Rate over VdIVW if 0.937ns>tCK≥0.625ns	-	-	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL(AC)	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL(AC)	0.2*srf1	9	0.2*srf1	9	0.2*srf1	9	0.2*srr1	9	0.2*srf1	9	V/ns	9,10

Note:

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around VcentDQ,midpoint after VREFDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER=1e-16 when the Rx mask is not violated.
2. Defined over the DQ internal VREF range 1.
3. Overshoot and undershoot specifications apply.
4. DQ input pulse signal swing into the receiver must meet or exceed VIHL(AC)min. VIHL(AC)min is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e., a valid TdiPW.
5. DQ minimum input pulse width defined at the VcentDQmidpoint.
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over VdiVW mask centered at VcentDQmidpoint. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
9. Input slew rate between VdiVW mask edge and VIHL(AC)min points.

10. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVWmin, VdiVWmax, and minimum slew rate limits, then either TdiVWmin or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

11.7 Command, Control, and Address Setup, Hold, and Derating

The total tIS(setup time) and tIH(hold time) required is calculated to account for slew rate variation by adding the data sheet tIS(base) values, the VIL(AC)/VIH(AC) points, and tIH(base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS(total setup time)=tIS(base)+ΔtIS. For a valid transition, the input signal has to remain above/ below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min.

Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

Table 11-5. Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	-	ps	VIH/L(AC)
tIH(base, DC75)	140	125	105	87	-	-	-	ps	VIH/L(DC)
tIS(base, AC90)	-	-	-	-	55	48	40	ps	VIH/L(AC)
tIH(base, DC65)	-	-	-	-	80	73	65	ps	VIH/L(DC)
tIS/tIH(VREF)	215	200	180	162	145	138	130	ps	

Note:

1. Base AC/DC referenced for 1V/ns slew rate and 2V/ns clock slew rate.
2. Values listed are referenced only; applicable limits are defined elsewhere.

Table 11-6. Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
VIH(AC)min	100	100	100	100	90	90	90	mV	VIH/L(AC)
VIH(DC)min	75	75	75	75	65	65	65	mV	VIH/L(DC)
VIL(DC)max	-75	-75	-75	-75	-65	-65	-65	mV	VIH/L(AC)
VIL(AC)max	-100	-100	-100	-100	-90	-90	-90	mV	VIH/L(DC)

Note:

1. Command, Address, Control input levels relative to VREFCA.

2. Values listed are referenced only; applicable limits are defined elsewhere.

Table 11-7. Derating Values DDR4-1600/1866/2133/2400 tIS/tIH - AC/DC Based

ΔtIS, ΔtIH derating in [ps] AC/DC Based(1)																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
ADDR, CNTL Input Slew Rate V/ns	7	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	**0**	**0**	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31

Note:

1. VIH/L(AC)=±100mV, VIH/L(DC)=±75mV; relative to VREFCA.

Table 11-8. Derating Values DDR4-2666/2933/3200 tIS/tIH - AC/DC Based

ΔtIS, ΔtIH derating in [ps] AC/DC Based(1)																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
ADDR, CNTL Input Slew Rate V/ns	7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	**0**	**0**	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Note:

1. VIH/L(AC)=±90mV, VIH/L(DC)=±65mV; relative to VREFCA.

12 Revision History

Version No	Description	Page	Date
1.0	Initial release	-	2025/3/21

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