

# **GSR6xx8xM**

# **DATASHEET**

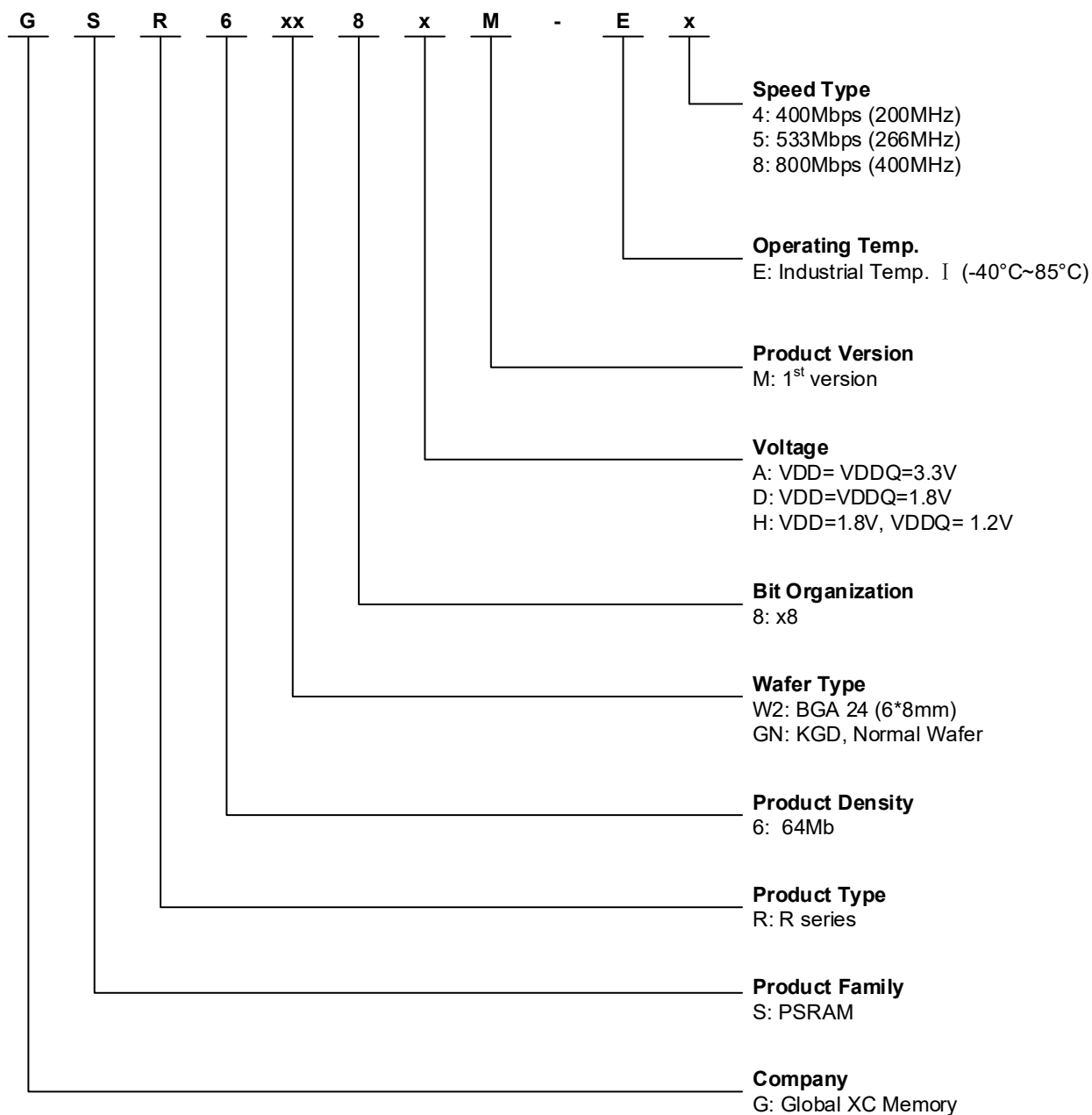
## Features

- ◆ 64M-bit DDR PSRAM
- ◆ Supply Voltage
  - 1.8V
    - VDD = 1.62V to 1.98V
    - VDDQ = 1.62V to 1.98V
  - 1.8V/1.2V
    - VDD = 1.62V to 1.98V
    - VDDQ = 1.14V to 1.26V
  - 3.3V
    - VDD = 2.7V to 3.6V
    - VDDQ = 2.7V to 3.6V
- ◆ Double-Data-Rate (DDR) Interface
  - 8-bit data bus
  - Two Bytes transfer per clock
  - Data mask (DM) for write operation
  - Data strobe (DQS) for high speed read operation
- ◆ Clock rate up to 400/200MHz for 1.8V/3.3V
  - 800/400MBps read/write throughput
- ◆ Organization
  - 8M x 8bits with 1024 Bytes per page
- ◆ Operating temperature range
  - Industrial Temp. I : -40°C to 85°C
  - Industrial Temp. II : -40°C to 105°C (TBD)
- ◆ Power Saving Features
  - Partial array self-refresh
  - Auto temperature compensated Self- Refresh
  - User configurable refresh rate
  - Low Power Mode (LPM) with Data Retention
- ◆ Low Power Consumption
  - 1.8V; 1.8V/1.2V
    - Typical 20μA in LPM with data retention (25°C)
    - Max 200μA standby current (85°C)
    - Max 13μA deep power down current (85°C)
  - 3.3V
    - Typical 30μA in LPM with data retention (25°C)
    - Max 250μA standby current (85°C)
    - Max 13μA deep power down current (85°C)
- ◆ Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst
  - 16/32/64/128/1K Bytes burst length
  - Hybrid burst
- ◆ Package Information
  - TFBGA-24ball (5x5 ball array)
  - KGD supported<sup>(1)</sup>

Note: For KGD and WLCSP information, please contact XC Memory regional sales for details

## Ordering Information

### Part Number Decoding



**Valid Part Numbers**
**Table 1. Valid Part Numbers**

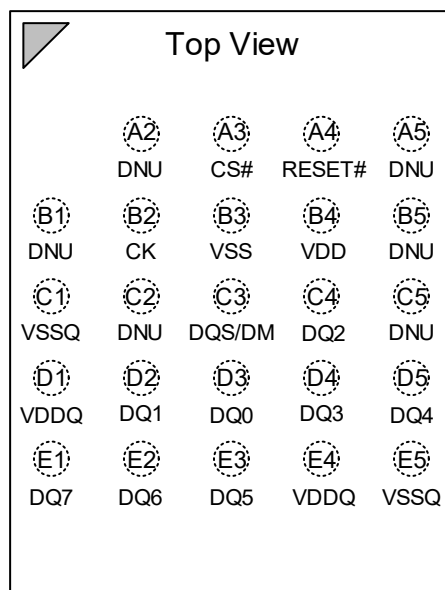
<b>Part Number</b>	<b>Voltage</b>	<b>Frequency</b>	<b>Temperature</b>	<b>Package</b>
GSR6GN8AM-E4	3.3V	200MHz	Tj=-40°C~85°C	KGD, Normal Wafer
GSR6GN8DM-E5	1.8V	266MHz	Tj=-40°C~85°C	KGD, Normal Wafer
GSR6GN8DM-E8	1.8V	400MHz	Tj=-40°C~85°C	KGD, Normal Wafer
GSR6GN8HM-E5	1.8V/1.2V	266MHz	Tj=-40°C~85°C	KGD, Normal Wafer
GSR6GN8HM-E8	1.8V/1.2V	400MHz	Tj=-40°C~85°C	KGD, Normal Wafer
GSR6W28AM-E4	3.3V	200MHz	Tc=-40°C~85°C	BGA24
GSR6W28DM-E5	1.8V	266MHz	Tc=-40°C~85°C	BGA24
GSR6W28DM-E8	1.8V	400MHz	Tc=-40°C~85°C	BGA24

## Contents

<b>1</b>	<b>PACKAGE INFORMATION .....</b>	<b>6</b>
1.1	BGA 24-BALL .....	6
1.2	PACKAGE OUTLINE DRAWING .....	7
<b>2</b>	<b>SIGNAL DESCRIPTION .....</b>	<b>8</b>
<b>3</b>	<b>BLOCK DIAGRAM .....</b>	<b>9</b>
<b>4</b>	<b>POWER-UP INITIALIZATION .....</b>	<b>10</b>
<b>5</b>	<b>INTERFACE DESCRIPTION .....</b>	<b>12</b>
5.1	ADDRESS SPACE .....	12
5.2	BURST TYPE AND LENGTH .....	12
5.3	COMMAND/ADDRESS LATCHING .....	12
5.4	COMMAND TRUTH TABLE .....	12
5.5	READ OPERATION .....	13
5.6	MULTI-COL READ OPERATION .....	15
5.7	MULTI-ROW READ OPERATION .....	16
5.8	WRITE OPERATION .....	16
5.9	MULTI-COL WRITE OPERATION .....	17
5.10	MULTI-ROW WRITE OPERATION .....	18
5.11	MODE REGISTERS .....	18
5.12	LOW POWER MODE .....	24
5.13	DEEP POWER DOWN MODE .....	25
5.14	SOFTWARE RESET .....	26
<b>6</b>	<b>ELECTRICAL SPECIFICATIONS .....</b>	<b>27</b>
6.1	ABSOLUTE MAXIMUM RATINGS .....	27
6.2	PIN CAPACITANCE-1.8V .....	27
6.3	PIN CAPACITANCE-3.3V .....	27
6.4	DECOUPLING CAPACITOR REQUIREMENT .....	28
6.5	OPERATING CONDITIONS .....	28
6.6	DC CHARACTERISTICS .....	29
6.7	ISB AND ILPM PARTIAL ARRAY REFRESH CURRENT-1.8V .....	30
6.8	ISB AND ILPM PARTIAL ARRAY REFRESH CURRENT-3.3V .....	31
6.9	AC CHARACTERISTICS .....	31
<b>7</b>	<b>REVISION HISTORY .....</b>	<b>33</b>

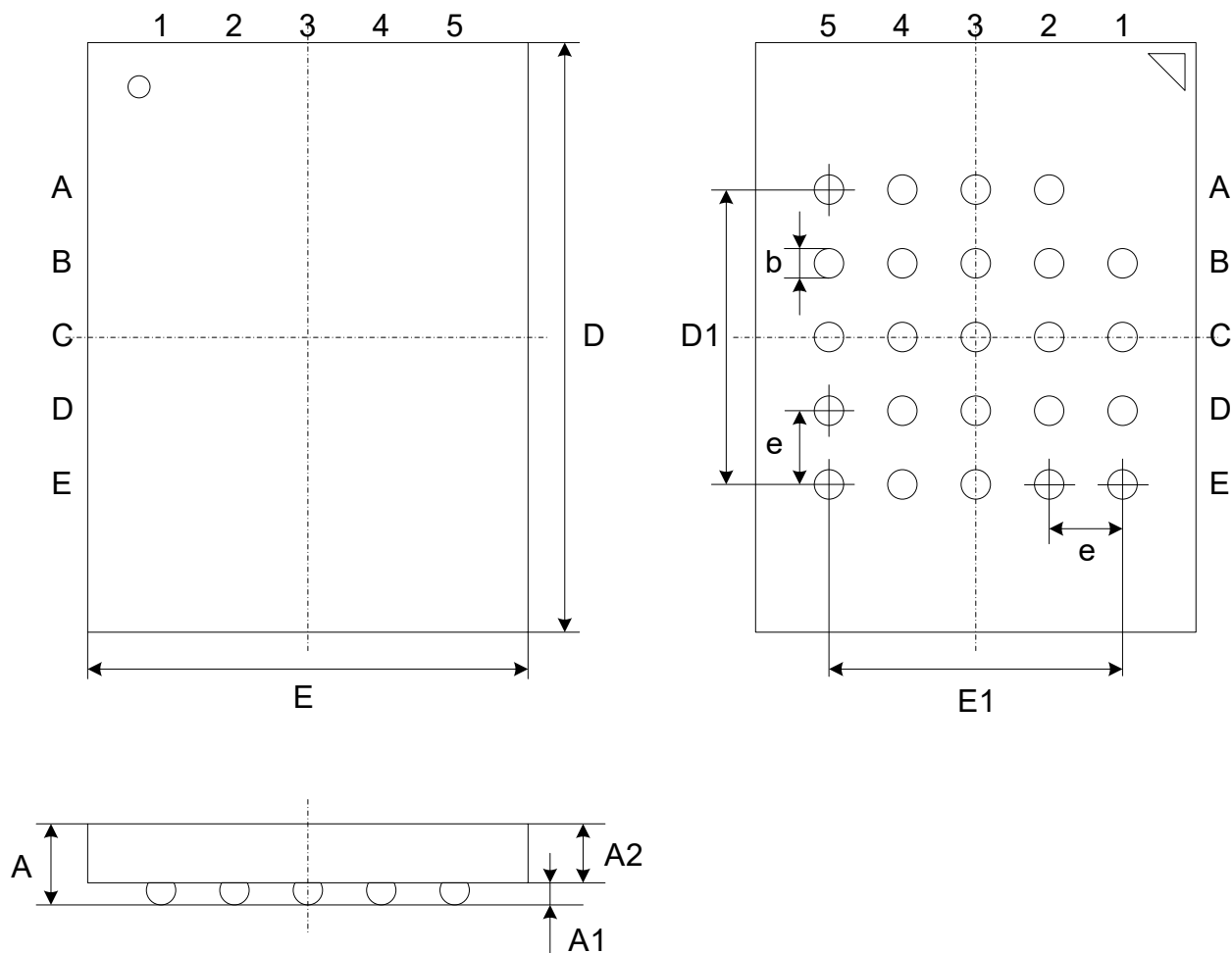
# 1 Package Information

## 1.1 BGA 24-ball



**Figure 1. Footprint for BGA 24-ball**

## 1.2 Package Outline Drawing



### Dimensions

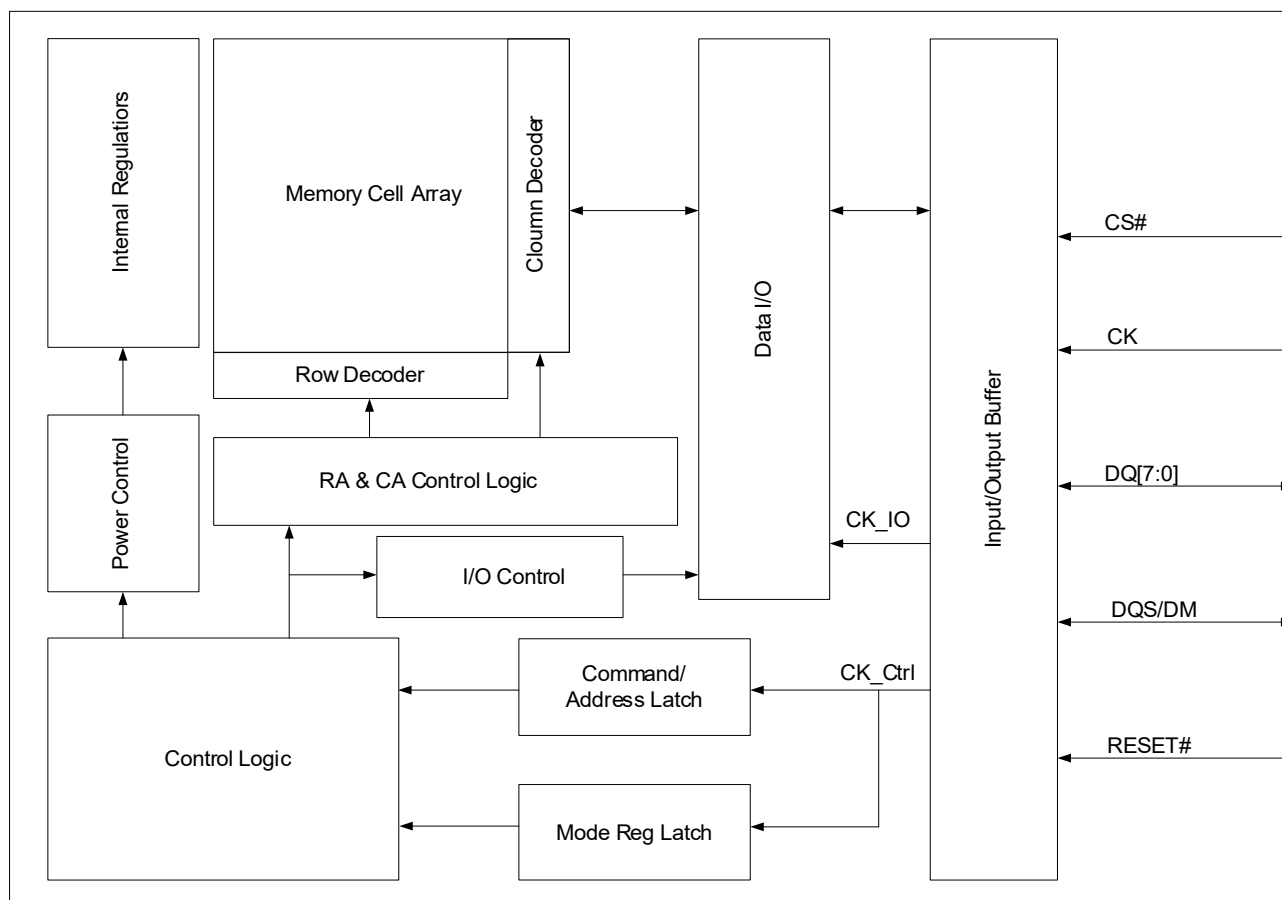
Symbol		A	A1	A2	b	E	E1	D	D1	e
Unit										
mm	Min	-	0.25	0.75	0.35	5.90	4.00 BSC	7.90	4.00 BSC	1.00 BSC
	Nom	-	0.30	0.80	0.40	6.00		8.00		
	Max	1.20	0.35	0.85	0.45	6.10		8.10		

## 2 Signal Description

Symbol	Type	Description	Note
VDD	Power	Core supply	
VDDQ	Power	IO supply	
VSS	Power	Core supply	
VSSQ	Power	IO supply	
DQ[7:0]	I/O	Data bus [7:0]	
DQS/DM	I/O	DQ strobe clock for DQ[7:0] during all reads. Data mask for DQ[7:0] during memory writes. DM is active high. DM=1 means "do not write".	
CS#	Input	Chip select	
CK	Input	Clock input	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	Not available for all package types



### 3 Block Diagram



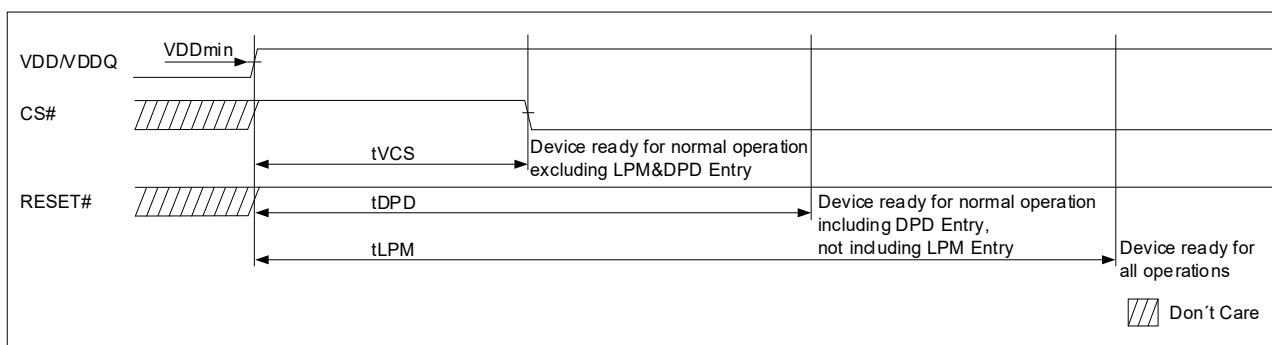
## 4 Power-Up Initialization

An on-chip voltage sensor is used to launch the power-up initialization process. VDD and VDDQ must be applied simultaneously. When the power supply reaches a stable level at or above VDD(min), the device will require tVCS time to complete its self-initialization process.

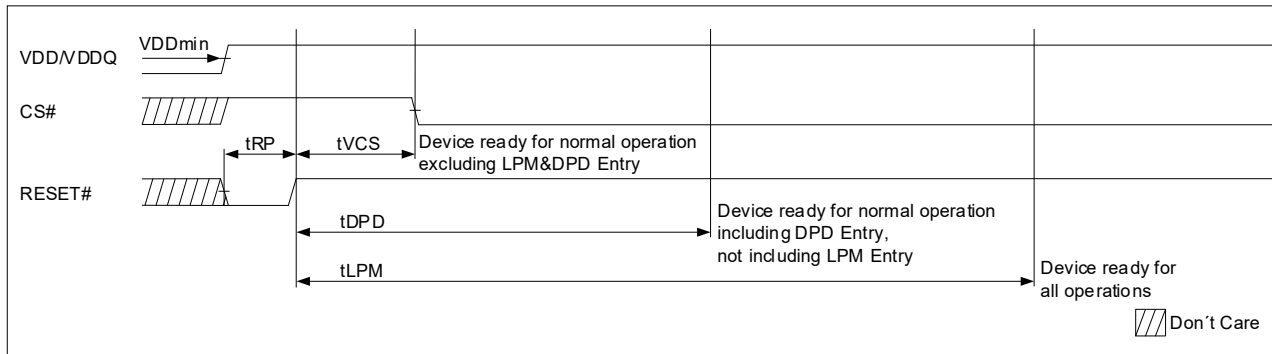
CS# should remain HIGH (track VDD within 200mV) and CLK should remain LOW during power-up.

If RESET# is LOW during power up, the device delays start of the tVCS period until RESET# is HIGH. The tVCS period is used primarily to perform refresh operations on the DRAM array to initialize it. When initialization is complete, the device is ready for normal operation.

For Deep Power Down entry, the device need tDPD time. For Low Power Mode, the device need tLPM time.

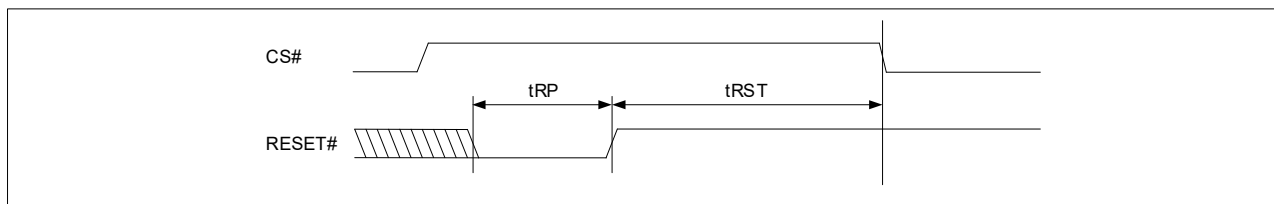


**Figure 2. Power-up with RESET# HIGH**



**Figure 3. Power-up with RESET# LOW**

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage is shown below.

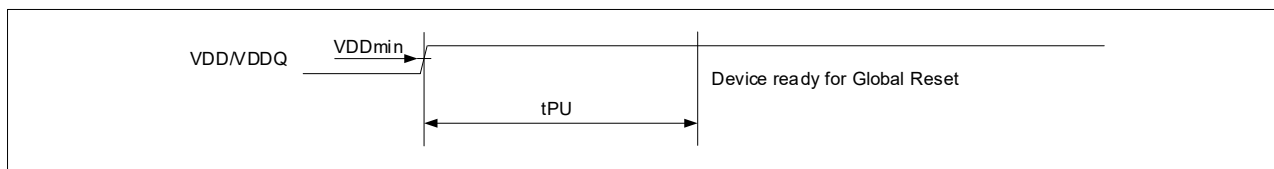


**Figure 4. RESET# Timing**

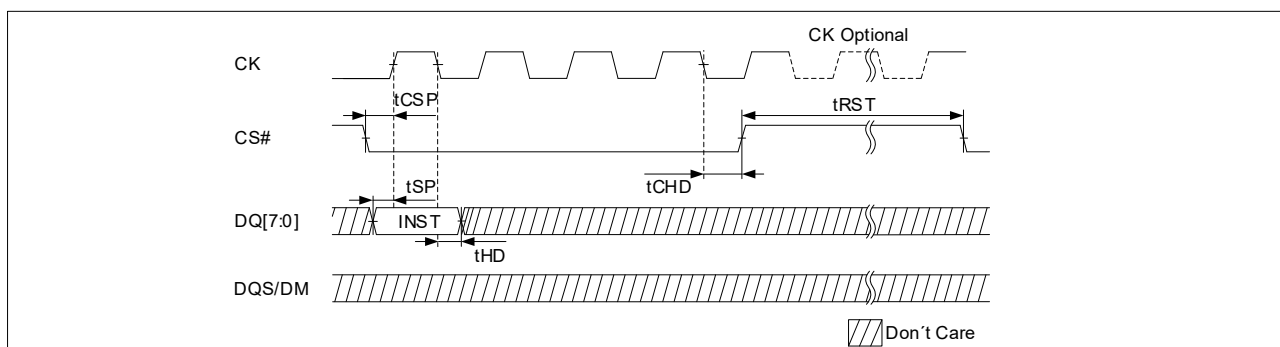
**Table 2. Power up and parameters**

Symbol	Parameter	Min	Max	Unit
tVCS	Power up reset time	150		$\mu$ s
tDPD	VDD/VDDQ $\geq$ min to Deep Power Down (DPD) entry	500		$\mu$ s
tLPM	VDD/VDDQ $\geq$ min to Low Power Mode (LPM) entry	1		ms

As an alternate power-up initialization method, After the tPU the Global Reset command is used to reset the device as follows:


**Figure 5. Power-Up Initialization by Global Reset**

The Global Reset command resets all register contents. Memory content is not guaranteed. Clocking is optional during tRST. Note that Global Reset command can be used ONLY as Power-up initialization.


**Figure 6. Global Reset Timing**

## 5 Interface Description

### 5.1 Address Space

Memory page size is 1K Byte. CA bits are used for data access within one page and RA bits are used for page addressing.

**Table 3. Address bits map-16bits based**

	X8			
	A3	A2	A1	A0
DQ7	0b	RA9	RA1	0b
DQ6	0b	RA8	RA0	0b
DQ5	0b	RA7	CA8	0b
DQ4	0b	RA6	CA7	0b
DQ3	0b	RA5	CA6	0b
DQ2	RA12	RA4	CA5	CA2
DQ1	RA11	RA3	CA4	CA1
DQ0	RA10	RA2	CA3	CA0

### 5.2 Burst Type and Length

Burst lengths of 16/32/64/128/1K Bytes in standard or hybrid wrap modes are register configurable. The device also includes command burst options for Linear Bursting. Bursts can start on any address. Write burst length requires a minimum of 2 Bytes. Read has no minimum length limit.

Both write and read have no restriction on maximum burst length as long as tCSM is met.

### 5.3 Command/Address Latching

After CS# goes LOW, instruction code is latched on 1<sup>st</sup> CK rising edge. Access address is latched on the 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup>, and 6<sup>th</sup> CK edges (1<sup>st</sup> falling edge, 2<sup>nd</sup> CK rising edge, 2<sup>nd</sup> CK falling edge, 3<sup>rd</sup> CK falling edge). For multi-col and multi-row access, more clocks are required for address latching.







### 5.4 Command Truth Table

The device recognizes commands listed in the following table. Instruction and address are input through DQ[7:0] pins. Host must send correct instruction and address format according to the following table.

Note that Linear Burst commands (20h and A0h) ignore burst setting defined by Mode Register.

Note that only Linear Burst Read command (A0h) is capable of performing row boundary crossing read.







**Table 4. Command Truth Table**

	1 <sup>st</sup> CK		2 <sup>nd</sup> CK		3 <sup>rd</sup> CK	
						
Sync Read	80h	A3	A2	A1	00h	A0
Sync Write	00h	A3	A2	A1	00h	A0
Linear Burst Read	A0h	A3	A2	A1	00h	A0
Linear Burst Write	20h	A3	A2	A1	00h	A0
Mode Register Read	C0h/E0h	00h	MA1	00h	00h	MA0
Mode Register Write	40h/60h	00h	MA1	00h	00h	MA0
Multi Column Burst Read	04h	A3	A2	A1	00h	A0
Multi Column Burst Write	84h	A3	A2	A1	00h	A0
Multi Row Burst Read	02h	A3	A2	A1	00h	A0
Multi Row Burst Write	82h	A3	A2	A1	00h	A0
Refresh	B0h	x	x	x	x	x
Global Reset	FFh	x	x	x	x	x

Note:

1. x = don't care
2. MA = Mode Register Address

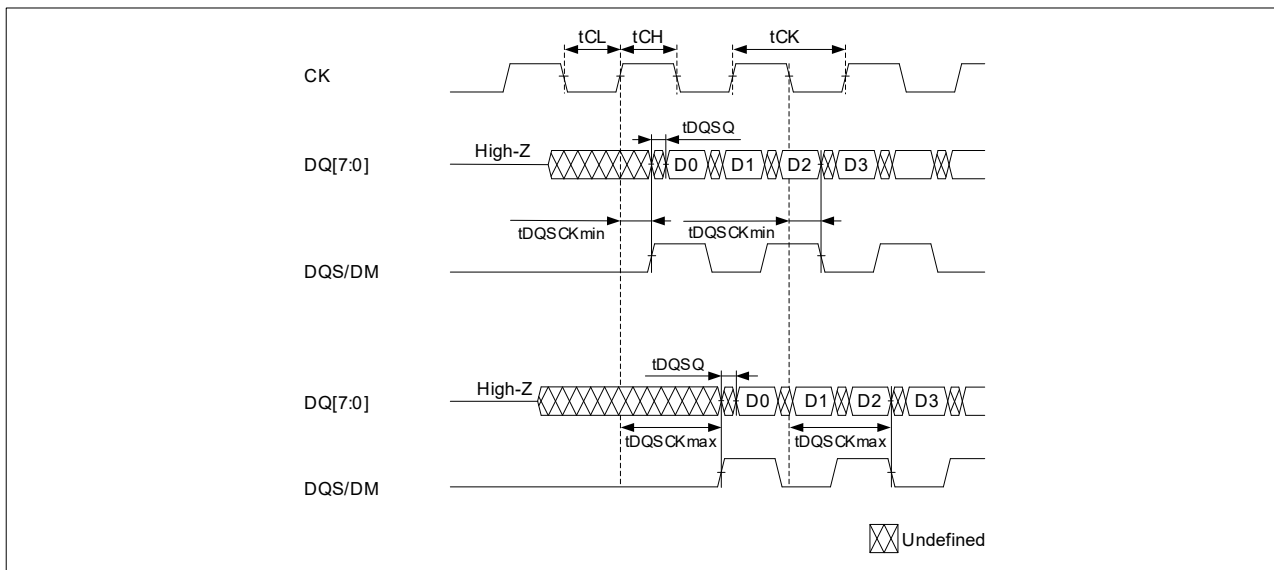
**Table 5. Command Truth Table (cont.)**

	4 <sup>th</sup> CK		5 <sup>th</sup> CK		6 <sup>th</sup> CK	
						
Multi Col Burst Read	A1 <sub>1</sub>	A0 <sub>1</sub>	A1 <sub>2</sub>	A0 <sub>2</sub>	A1 <sub>3</sub>	A0 <sub>3</sub>
Multi Col Burst Write	A1 <sub>1</sub>	A0 <sub>1</sub>	A1 <sub>2</sub>	A0 <sub>2</sub>	A1 <sub>3</sub>	A0 <sub>3</sub>
Multi Row Burst Read	A3 <sub>1</sub>	A2 <sub>1</sub>	A1 <sub>1</sub>	A0 <sub>1</sub>	x	x
Multi Row Burst Write	A3 <sub>1</sub>	A2 <sub>1</sub>	A1 <sub>1</sub>	A0 <sub>1</sub>	x	x

## 5.5 Read Operation

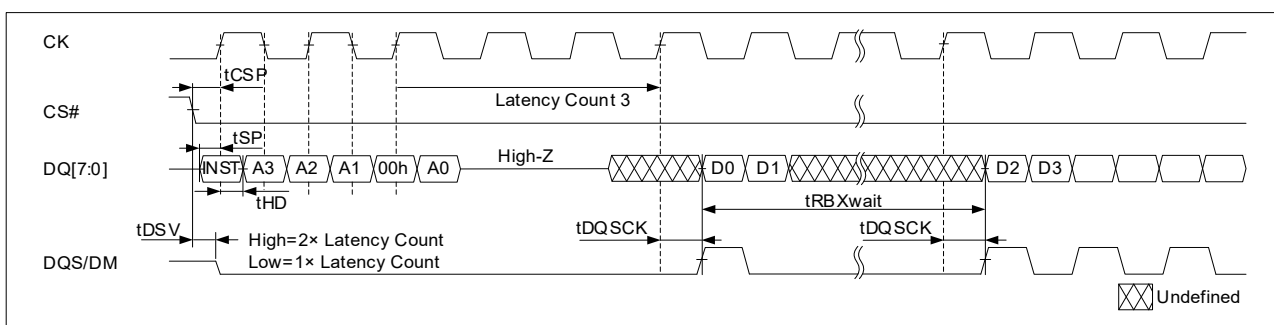
Output data is available after Command/Address latching and latency cycles. Latency cycle configuration is defined in Mode Register. For fixed latency setting, the latency length is LCx2. For variable latency setting, DQS/DM indicates the latency count. If DQS/DM is LOW during the Command/Address cycles, latency length is LCx1. If DQS/DM is HIGH during the Command/Address cycles, an additional LC is inserted and the total latency length is LCx2. After Command/Address latching, the device initializes DQS/DM to 0. Once these latency clocks have been completed the memory starts to simultaneously transition DQS/DM and output the target data.





**Figure 10. Read DQS/DM & DQ Timing**

When Linear Burst Read Command (A0h) is issued, read operation may cross row boundaries as shown below.

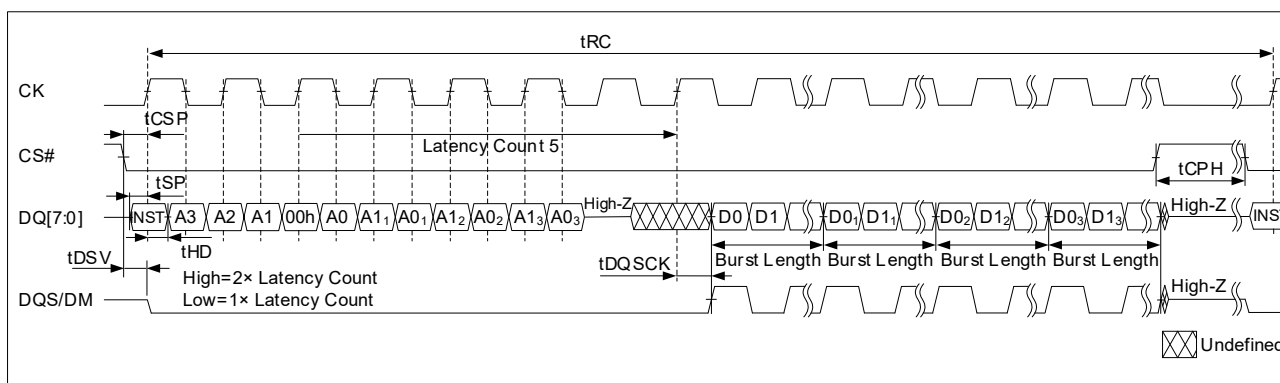


**Figure 11. Linear Burst Read with Row Boundary Crossing (Starting Column address 1FFh)**

## 5.6 Multi-Col Read Operation

Multi column read function is used for random read in one row, which significantly improves the I/O efficiency by saving time expense of instruction/address input, latency clocks and tCPH.

After inputting instruction code (04h) and first address (A3, A2, A1, A0), the same timing as Read operation, 3 additional column addresses (A1<sub>1</sub>, A0<sub>1</sub>, A1<sub>2</sub>, A0<sub>2</sub>, A1<sub>3</sub>, A0<sub>3</sub>) should be input in sequence. The data of the first column address is available after LC latency cycles. Note that LC setting is different from normal read operation, as shown in Table 12. The data output length of each address is defined by MR2-Byte1[1:0], and CA[1:0] should be 00b. Note that burst length must NOT be set as 1K-Byte (MR2-Byte0[0]≠0b).

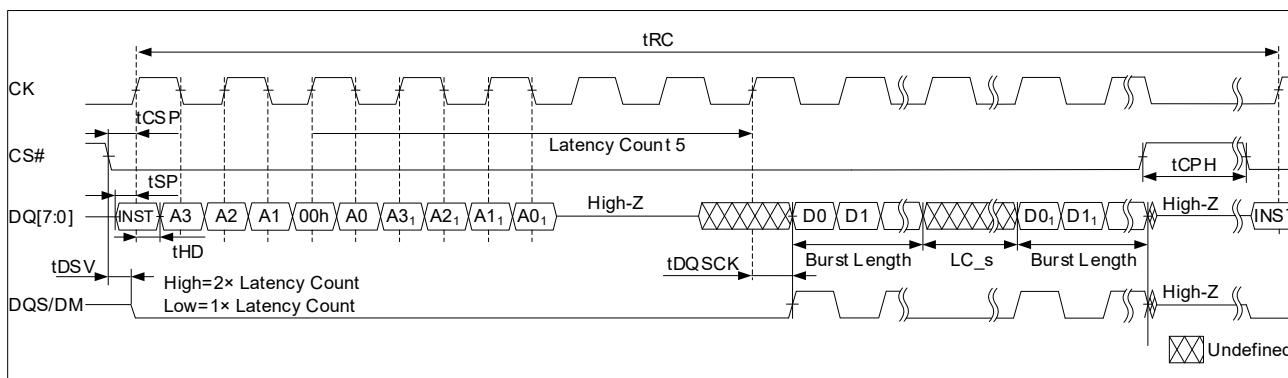


**Figure 12. Multi-Col Read Timing**

## 5.7 Multi-Row Read Operation

Multi row read function is used for random read in different rows, which is an efficient way to saving time expense of instruction/address input, latency clocks and tCPH for random access.

After inputting instruction code (02h) and first address (A3, A2, A1, A0), the same timing as Read operation, one additional address (A3<sub>1</sub>, A2<sub>1</sub>, A1<sub>1</sub>, A0<sub>1</sub>) should be input in sequence. The data of the first address is available after LC latency cycles. Note that LC setting is different from normal read operation, as shown in Table 12. The data output length of each address is defined by MR2-Byte1[7:4]. Following data out of the first address and a shorter latency (LC<sub>s</sub>), the data of the second address is output. The latency count is set by MR2-Byte1[7:4]. Note that burst length must NOT be set as 1K-Byte (MR2-Byte0[0]≠0b).



**Figure 13. Multi-Row Read Timing**

## 5.8 Write Operation

A minimum of 2 Bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CS# high time between operations. Single-Byte write operations can be done by masking through DQS/DM pin.

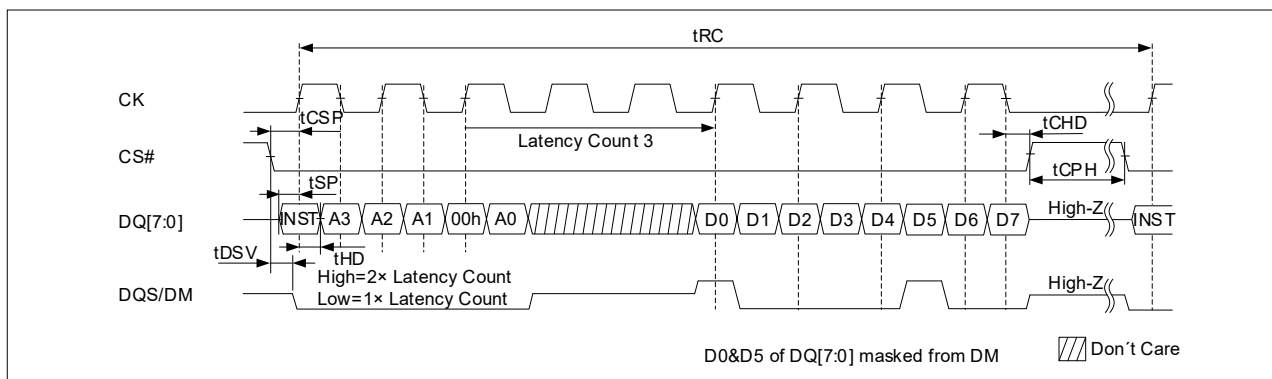
Data will continue to be transferred as long as the master continues to transition the clock while CS# is LOW. Note that burst transactions should not be so long as to prevent the memory from doing distributed refreshes.

Wrapped bursts will continue to wrap within the burst length. Hybrid wrap will wrap once then switch to linear burst starting at the next wrap boundary. Linear burst will wrap at the page edge. A maximum of 1K Byte of data could be input by a single Linear Write command. Write transfers can be ended at any time by bringing CS# HIGH when the clock is idle.

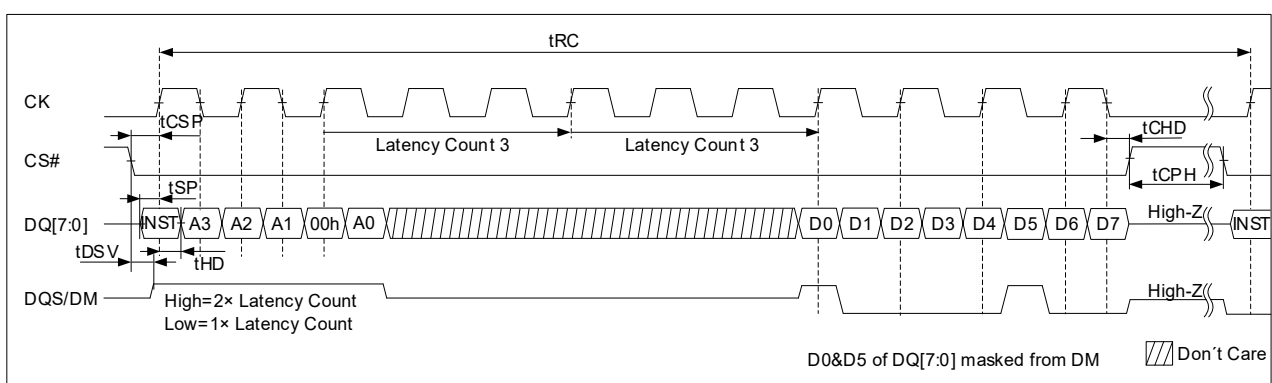
For variable latency setting, DQS/DM indicates the latency length. If DQS/DM is LOW during the Command/Address cycles,



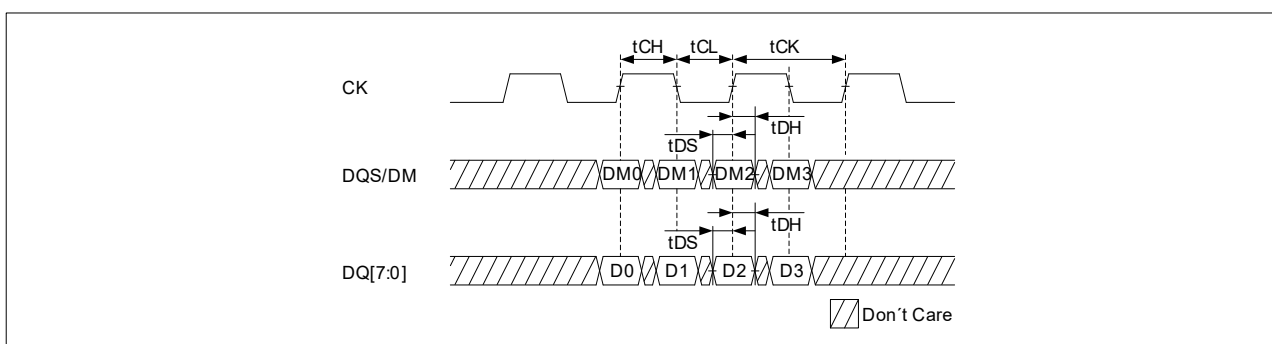
latency count LCx1. If DQS/DM is HIGH during the Command/Address cycles, an additional latency is inserted and the total latency count is LCx2.



**Figure 14. Write Operation Timing (LCx1)**



**Figure 15. Write Operation Timing (LCx2)**



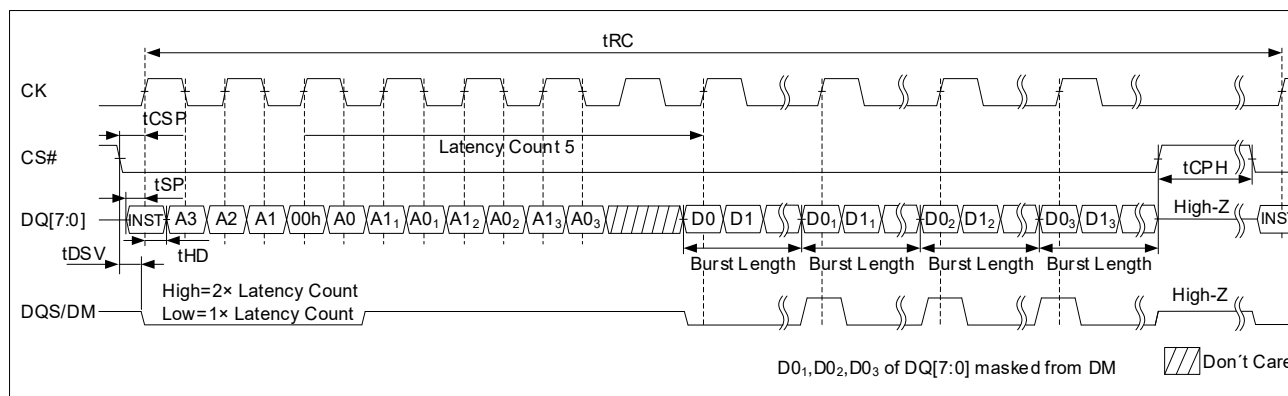
**Figure 16. Write DQS/DM & DQ Timing**

## 5.9 Multi-Col Write Operation

Multi column write function is used for random write in one row, which significantly improves the I/O efficiency by saving time expense of instruction/address input, latency clocks and tCPH.

After inputting instruction code (84h) and first address (A3, A2, A1, A0), the same timing as Write operation, 3 additional column addresses (A1<sub>1</sub>, A0<sub>1</sub>, A1<sub>2</sub>, A0<sub>2</sub>, A1<sub>3</sub>, A0<sub>3</sub>) should be input in sequence. CA[1:0] of each address should be 00b. Each column address should be input in sequence after LC latency cycles. Note that LC setting is different from normal read operation, as shown in Table 12. Data length follows the setting in MR2-Byte1[1:0], and the data of the 4 column address is

input successively. Note that burst length must NOT be set as 1K-Byte (MR2-Byte0[0]≠0b).

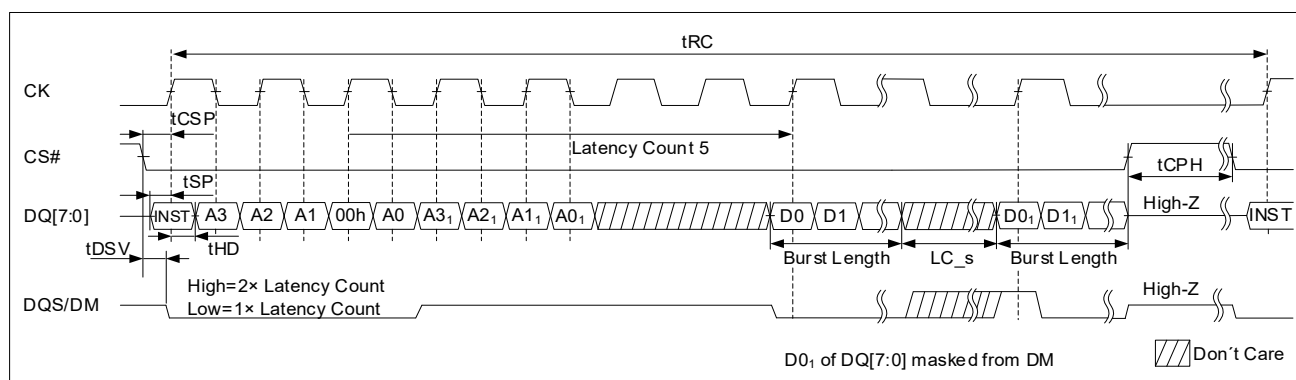


**Figure 17. Multi-Col Write Timing**

## 5.10 Multi-Row Write Operation

Multi row write function is used for random write in different rows, which is an efficient way to save time expense of instruction/address input, latency clocks and tCPH for random access.

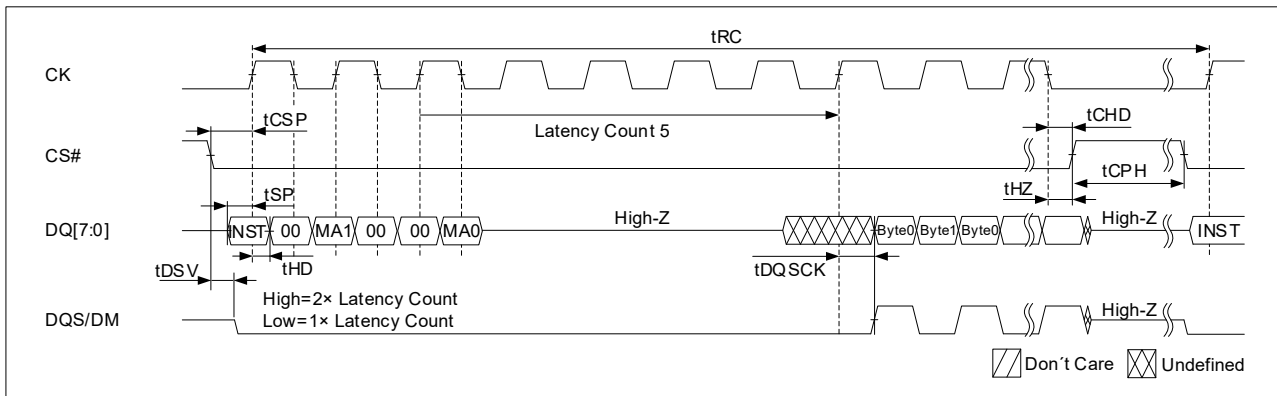
After inputting instruction code (82h) and first address (A3, A2, A1, A0), the same timing as Write operation, one additional address (A3<sub>1</sub>, A2<sub>1</sub>, A1<sub>1</sub>, A0<sub>1</sub>) should be input in sequence. The data of the first address should be input after LC latency cycles. A shorter latency (LC<sub>s</sub>) is insert between each data burst. The LC count is set by MR2-Byte1[7:4]. Note that LC setting is different from normal read operation, as shown in Table 12. Data length follows the setting in MR2-Byte1[1:0], and CA[1:0] should be 00b. Note that burst length must NOT be set as 1K-Byte (MR2-Byte0[0]≠0b).



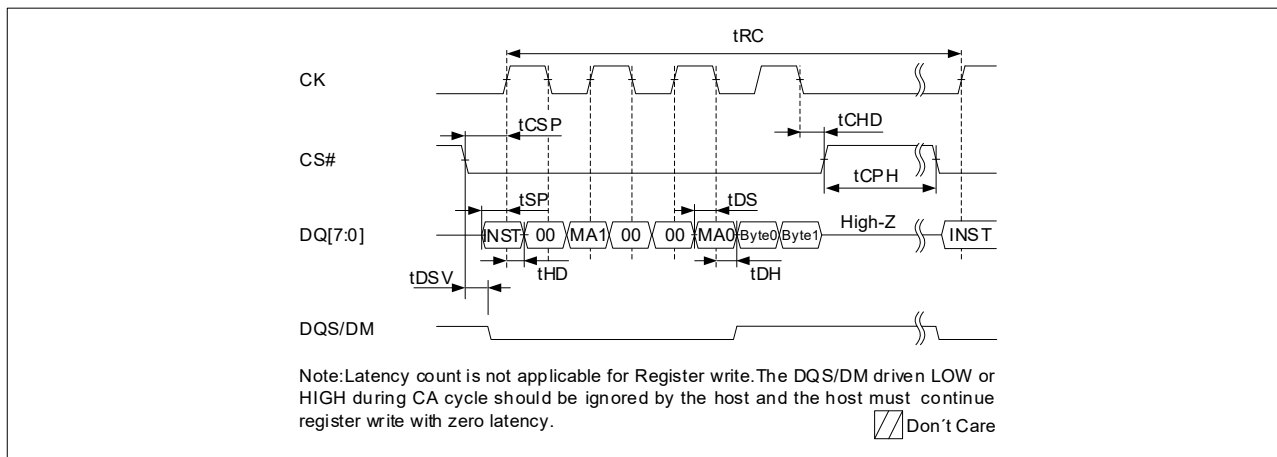
**Figure 18. Multi-Row Write Timing**

## 5.11 Mode Registers

Mode Register Read Timing is shown below. Mode Register Address in command determines which Mode Register is read from. All Mode Registers are 16-bit wide and transferred in one clock cycle (each 8-bit for rising edge and falling edge).


**Figure 19. Mode Register Read**

Register Writes are always latency 1. Latency Code (MR2-Byte1[7:4]) does not apply to Mode Register Write. Mode Register Read follow the same read latency settings, defined in MR2-Byte1[7:4]. MR1 and MR0 are read only. MR3 and MR2 are writable.


**Figure 20. Mode Register Write**
**Table 6. Mode Register Table**

MR No.	MA1 [31:24]	MA0. [7:0]	Access	Byte	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	00h	00h	R	Byte0				Row Address bit Count				
				Byte1	Column Address bit Count				Vendor ID(0000b)			
MR1	00h	01h	R	Byte0								
				Byte1	KGD				Device ID			
MR2	01h	00h	R/W	Byte0	DPD	Dr. Str.						B. Len.
				Byte1	Latency Code				LC T.	Burst T.	Burst Length	
MR3	01h	01h	R/W	Byte0	Software Reset					M. Ref.	Ref. Freq. Set	
				Byte1			LPMen	PASR			Ref. Freq. Flag	

Note:

- Blank box = reserved. The reserved bits should be set to 1b for MR[3:2].
- Addr.[23:8] should be 0000h.

**Table 7. Row Address bit Count MR0-Byte0[4:0] and Column Address bit Count MR0-Byte1[7:4]**

Density.	Row Addr. Count	MR0-Byte0[4:0]	Col. Addr. Count	MR0-Byte1[7:4]
64Mb	13	01100b	9	1000b

**Table 8. KGD Code MR1-Byte1[7]**

MR1-Byte1[7]	Description
0b	Good die
1b	Fail die

**Table 9. Device ID MR1-Byte1[3:0]**

MR1-Byte1[3:2]	Description
00b	VDD=VDDQ=1.8V
01b	VDD=1.8V, VDDQ= 1.2V
10b	VDD=VDDQ=3.3V
MR1-Byte1[1:0]	Description
00b	Device Without On-die ECC
01b	Device With On-die ECC

**Table 10. Deep Power Down Mode MR2-Byte0[7]**

MR2-Byte0[7]	Description
0b	Enter Deep Power Down Mode
1b	Normal Mode (default)

**Table 11. Drive Strength (Dr. Str.) Codes MR2-Byte0[6:4]**

MR2-Byte0[6:4]	Drive Strength (Dr. Str.)
000b	33 Ohms (default)
001b	100 Ohms
010b	66 Ohms
011b	50 Ohms
100b	40 Ohms
101b	25 Ohms
110b	20 Ohms
111b	reserved

**Table 12. Read/Write Latency Code MR2-Byte1[7:4]**

	Read Latency		Multi Col/Row Read Latency				Frequency
	LC_min	LC_max	LC_min	LC_max	Latency between data burst (LC_s)		
					Read	Write	
1110b	3	6	6	6	0	4	84MHz
1111b	4	8	6	8	0	5	108MHz
0000b	5	10	6	10	0	6	133MHz
0001b	6	12	6	12	0	8	166MHz
0010b	7	14	7	14	0	9	200MHz
0011b	8	16	8	16	0	10	213MHz
0100b	9	18	9	18	3	11	233MHz
0101b	10	20	10	20	4	13	266MHz
0110b	11	22	11	22	5	14	333MHz
0111b	12	24	12	24	6	16	400MHz
Others	Reserved						

Note:

1. Default setting is 0010b

The device is built with volatile DRAM array which requires periodic refresh of all bits in it. The refresh operation can be done by an internal self-refresh logic that will evenly refresh the memory array automatically. The automatic refresh operation can only be done when the memory array is not actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will insert additional latency time at the start of the new access in order to allow the refresh operation to complete before starting the new access.

**Table 13. Latency Type (LC T.) MR2-Byte1[3]**

MR2-Byte1[3]	Latency Type (LC T.)
0b	Variable
1b	Fixed (default)

**Table 14. Operation Latency**

Area	Operation	Refresh or not	Variable Latency	Fixed Latency
Memory	Read	No Refresh	LC	LCx2
		Refresh	LCx2	LCx2
	Write	No Refresh	LC	LCx2
		Refresh	LCx2	LCx2
Register	Read	No Refresh	LC	LCx2
		Refresh	LCx2	LCx2
	Write	Either	1	1

**Table 15. Burst Type (Burst T.) MR2-Byte1[2], Burst Length MR2-Byte0[0], MR2-Byte1[1:0]**

MR2-Byte0[0]	MR2-Byte1[2:0]	Burst Length
1b	000b	128 Byte Hybrid Wrap
1b	001b	64 Byte Hybrid Wrap
1b	010b	16 Byte Hybrid Wrap
1b	011b	32 Byte Hybrid Wrap
1b	100b	128 Byte Wrap
1b	101b	64 Byte Wrap
1b	110b	16 Byte Wrap
1b	111b	32 Byte Wrap (default)
0b	x11b	1K Byte Wrap

Note:

- For Multi-row and multi-column READ/WRIT, burst length must NOT be set as 1K-Byte (MR2-Byte0[0]≠0b).

Device powers up in 32 Byte Wrap. For non-Hybrid burst (MR2-Byte1[2]=1b), MR2-Byte1[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR2-Byte1[2]=0b), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (1k Byte) before wrapping around within the entire column address space. Burst length can be set to 16/32/64/128/1K Bytes.

**Table 16. Example of Wrap/Hybrid Wrap**

MR2-Byte0[0]	MR2-Byte1[2:0]	Starting	Burst Address Sequence
1b	000b	2	2,3,4,...63,0,1,64,65,66...
1b	001b	2	2,3,4,...31,0,1,32,33,34...
1b	010b	2	2,3,4,5,6,7,0,1,8,9,10...
1b	011b	2	2,3,4,...15,0,1,16,17,18...
1b	100b	4	[4,5,6,...63,0,1,2,3]
1b	101b	4	[4,5,6,...31,0,1,2,3]
1b	110b	4	[4,5,6,7,0,1,2,3]
1b	111b	4	[4,5,6,...15,0,1,2,3]
0b	x11b	4	[4,5,6,...511,0,1,2,3]

The Linear Burst Commands (20h and A0h) ignore the wrap settings(MR8[2:0]). Linear Burst Read (A0h) can cross page edge. Linear Burst Write (20h) cannot cross page edge.

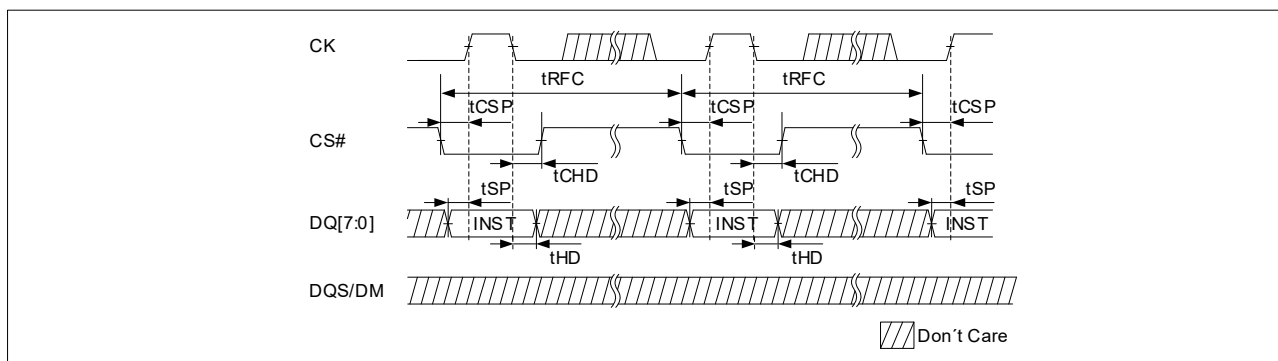
**Table 17. Software Reset MR3-Byte0[7:4]**

MR3-Byte0[7:4]	Description
1010b	Software Reset
1111b	Default
Others	Reserved

**Table 18. Manual Refresh MR3-Byte0[2]**

MR3-Byte0[2]	Manual Refresh Setting
0b	Manual Refresh enabled
1b	Manual Refresh disabled (default)

When Manual Refresh is enabled, the controller takes accountability of array refresh by issuing Refresh command (opcode B0h). The duration of Refresh is  $t_{RFC}$ , within which no instruction is allowed. At least 1024 Refresh command is required within  $t_{REFW}$ . Burst refresh up to 1024 is allowed


**Figure 21. Refresh Timing**

When Manual Refresh is disabled, the distributed refresh operation requires that the host does not perform burst transactions longer than the distributed refresh interval to prevent the memory from doing the distributed refreshes operation when it is needed. This sets an upper limit on the length of read and write transactions so that the automatic distributed refresh operation can be done between transactions. This limit is called the CS# low maximum time ( $t_{CSM}$ ) and  $t_{CSM}$  will be equal to the maximum distributed refresh interval. The host system is required to respect the  $t_{CSM}$  value by terminating each transaction before violating  $t_{CSM}$ . This can be done by host memory controller splitting long transactions when reaching the  $t_{CSM}$  limit, or by host system hardware or software not performing a single burst read or write transaction that would be longer than  $t_{CSM}$ . The maximum refresh interval is longer at lower temperatures such that  $t_{CSM}$  could be increased to allow longer transactions.

**Table 19. Refresh Frequency Setting MR3-Byte0[1:0]**

MR3-Byte0[1:0]	Refresh Frequency Setting
00b	Enable 0.5x Refresh when temperature allows
01b	Enable 1x Refresh when temperature allows
10b	reserved
11b	Always 4x Refresh (default)

**Table 20. Low Power Mode (LPM) enable MR3-Byte1[5]**

MR3-Byte1[5]	Description
0b	Normal Mode (default)
1b	Enter Low Power Mode

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only part of the memory array required by the host system. The refresh options are full array,

one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

**Table 21. Partial Array Self-Refresh (PASR) Setting MR3-Byte1[4:2]**

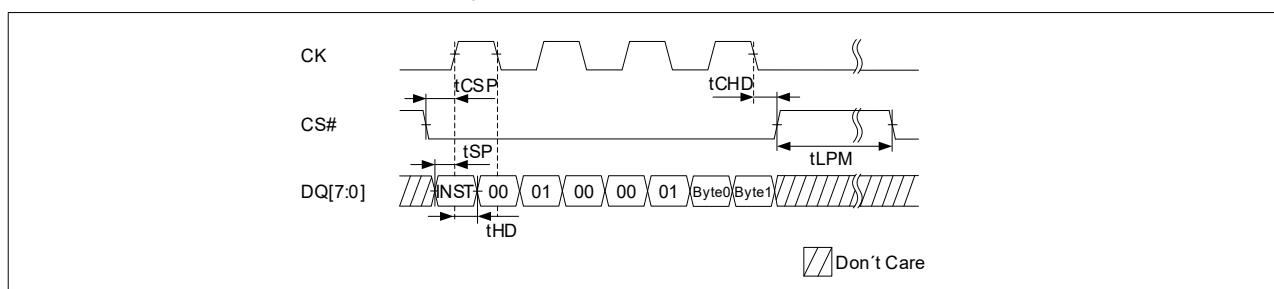
MR3-Byte1[4:2]	Refresh Range
000b	Full array (default)
001b	Bottom 1/2 array
010b	Bottom 1/4 array
011b	Bottom 1/8 array
100b	None
101b	Top1/2 array
110b	Top1/4 array
111b	Top1/8 array

**Table 22. Self Refresh Flag (Read-Only) MR3-Byte1[1:0]**

MR3-Byte1[1:0]	Self Refresh Interval
00b	0.5x Refresh (tCSM=8μs)
01b	1x Refresh (tCSM=4μs)
10b	4x Refresh (tCSM=1μs)
11b	reserved

## 5.12 Low Power Mode

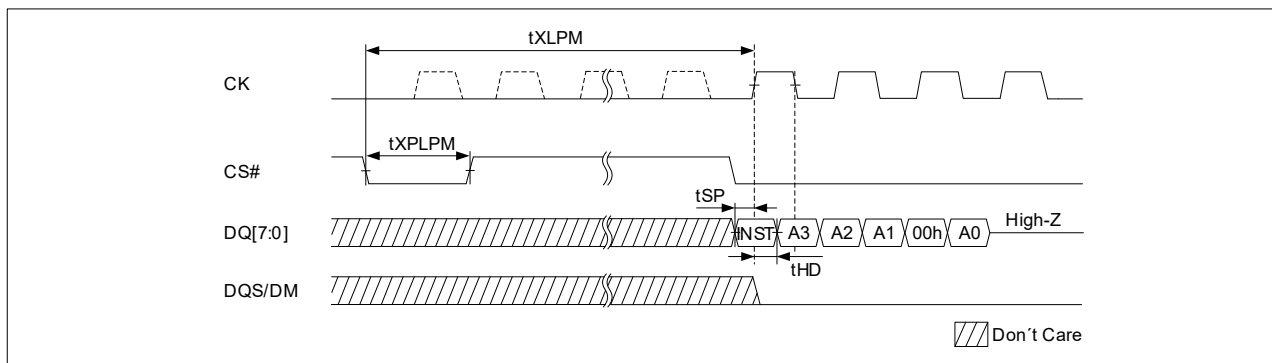
Low Power Mode puts the device in an ultra-low power state, while the stored data is retained. Low Power Mode Entry is by writing 1b into MR3-Byte1[5]. CS# going high initiates the Low Power mode and must be maintained for the minimum duration of tLPM. The Low Power Mode Entry command sequence is shown below.



**Figure 22. Low Power Mode Entry**

Low Power Mode Exit is initiated by a low pulsed CS#. Afterwards, CS# can be held high with or without clock toggling until the first operation begins (observing minimum Low Power Mode Exit time, tXLPM).

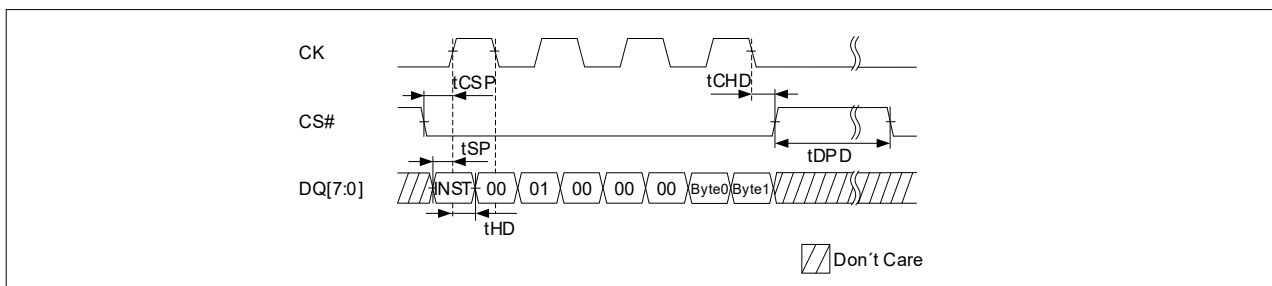




**Figure 23. Low Power Mode Exit (Read Operation shown as example)**

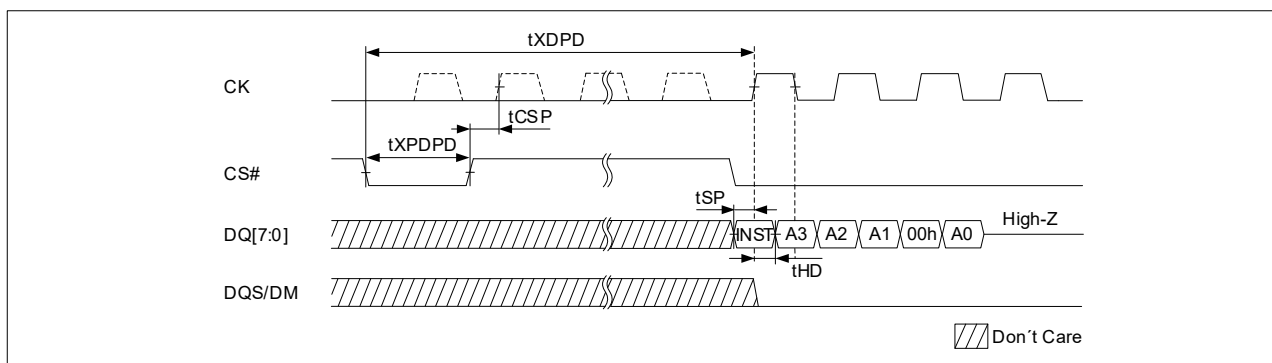
### 5.13 Deep Power Down Mode

Deep Power Down Mode (DPD) puts the device into power down state. DPD Mode Entry is entered by writing 0b into MR2-Byte0[7]. CS# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.



**Figure 24. Deep Power Down Entry**

Deep Power Down Exit is initiated by a low pulsed CS#. After a CS# DPD exit, CS# must be held high with or without clock toggling until the first operation begins (observing minimum Deep Power Down Exit time, tXDPD).

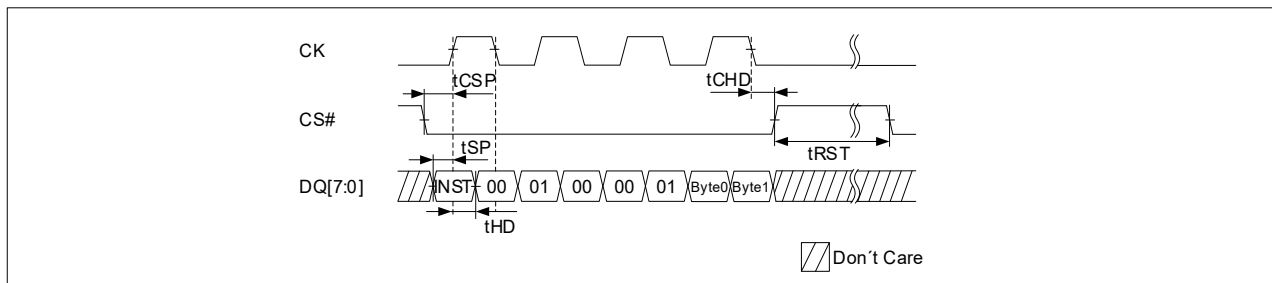


**Figure 25. Deep Power Down Exit (Read Operation shown as example)**

Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial power up to the first DPD entry.

## 5.14 Software Reset

The Software Reset provides a software method of returning the device to the standby state. During  $t_{RST}$  the device will draw  $I_{RST}$  current. While Software Reset time ( $t_{RST}$ ), bus transactions are not allowed. Register values and memory content are not retained after Software Reset, and register values will reset to defaults.



**Figure 26. Software Reset Timing**

## 6 Electrical Specifications

### 6.1 Absolute Maximum Ratings

**Table 23. Absolute Maximum Ratings**

Symbol	Parameter	Rating	Unit	Note
VT	Voltage to any ball except VDD, VDDQ relative to VSS	-0.4 to VDD/VDDQ+0.4	V	
VDD	Voltage on VDD supply relative to VSS	-0.4 to +2.45	V	For 1.8V
		-0.4 to +4	V	For 3.3V
VDDQ	Voltage on VDDQ supply relative to VSS	-0.4 to +2.45	V	For 1.8V
		-0.4 to +4	V	For 3.3V
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C	1

Note:

- Storage temperature refers to the case surface temperature on the center/top side of the PSRAM

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 6.2 Pin Capacitance-1.8V

**Table 24. Bare Die Pin Capacitance (T<sub>A</sub> = 25°C)**

Symbol	Parameter	Min	Max	Unit	Note
CIN	Input Pin Capacitance		1	pF	VIN=0V
COUT	Output Pin Capacitance		2	pF	VOUT=0V

**Table 25. Package Pin Capacitance (T<sub>A</sub> = 25°C)**

Symbol	Parameter	Min	Max	Unit	Note
CIN	Input Pin Capacitance		5	pF	VIN=0V
COUT	Output Pin Capacitance		6	pF	VOUT=0V

**Table 26. Load Capacitance**

Symbol	Parameter	Min	Max	Unit	Note
CL	Load Capacitance		15	pF	≤200Mhz
			10	pF	>200Mhz

Note:

- System CL for the use of package

### 6.3 Pin Capacitance-3.3V

**Table 27. Bare Die Pin Capacitance (T<sub>A</sub> = 25°C)**

Symbol	Parameter	Min	Max	Unit	Note
CIN	Input Pin Capacitance		2	pF	VIN=0V
COUT	Output Pin Capacitance		3	pF	VOUT=0V

**Table 28. Package Pin Capacitance ( $T_A = 25^\circ\text{C}$ )**

Symbol	Parameter	Min	Max	Unit	Note
CIN	Input Pin Capacitance		6	pF	VIN=0V
COUT	Output Pin Capacitance		8	pF	VOUT=0V

**Table 29. Load Capacitance**

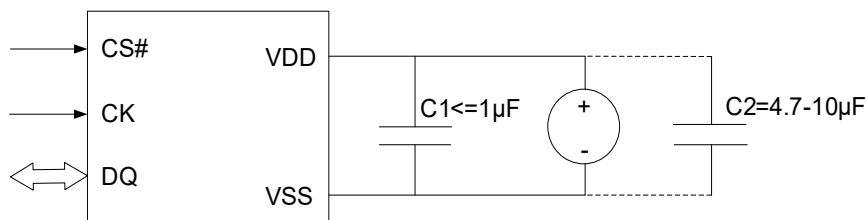
Symbol	Parameter	Min	Max	Unit	Note
CL	Load Capacitance		15	pF	$\leq 200\text{Mhz}$

Note:

1. System CL for the use of package

## 6.4 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



### Low ESR cap C1

It is recommended to place a low ESR decoupling capacitor of  $\leq 1\mu\text{F}$  close to the device to absorb transient peaks.

### Large cap C2

Though Low Power Mode average current is small (less than  $100\mu\text{A}$ ), its peak current from internal periodical burst refresh can reach up to the level of  $25\text{mA}$ . The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a  $4.7\mu\text{F}$ - $10\mu\text{F}$  cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh. Contact XC Memory for further decoupling solution assistance.

## 6.5 Operating Conditions

**Table 30. Operating Temperature**

Parameter	Min	Max	Unit
Operating Temperature (Industrial Temp. I )	-40	85	$^\circ\text{C}$
Operating Temperature (Industrial Temp. II )	-40	105	$^\circ\text{C}$

## 6.6 DC Characteristics

**Table 31. DC Characteristics-1.8V**

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{DD}$	Supply Voltage	1.62		1.98	V	
$V_{DDQ}$	I/O Supply Voltage ( $V_{DDQ}=1.8V$ )	1.62		1.98	V	
	I/O Supply Voltage ( $V_{DDQ}=1.2V$ )	1.14		1.26	V	
$V_{IH}$	Input high voltage	$V_{DDQ} - 0.4$		$V_{DDQ} + 0.2$	V	
$V_{IL}$	Input low voltage	-0.2		0.4	V	
$V_{OH}$	Output high voltage ( $I_{OH}=-0.2mA$ )	$0.8 V_{DDQ}$			V	
$V_{OL}$	Output low voltage ( $I_{OL}=+0.2mA$ )			$0.2 V_{DDQ}$	V	
$I_{LI}$	Input Pin leakage current	-1		1	$\mu A$	
$I_{LO}$	Output Pin leakage current	-1		1	$\mu A$	
$I_{DD}$	Read @166MHz		17	19	mA	1,2
	Read @200MHz		20	22	mA	1,2
	Read @266MHz		22	25	mA	1,2
	Read @333MHz		29	33	mA	1,2
	Read @400MHz		35	38	mA	1,2
$I_{DD}$	Write @166MHz		16	18	mA	1,2
	Write @200MHz		18	20	mA	1,2
	Write @266MHz		20	23	mA	1,2
	Write @333MHz		25	27	mA	1,2
	Write @400MHz		31	35	mA	1,2
$I_{SB}$	Standby current (-40 to 85°C)		66	200	$\mu A$	1,2,3,4,5
$I_{DPD}$	Deep Power Down current		4	13	$\mu A$	1,2,3
$I_{RST}$	Software Reset current		70	250	$\mu A$	1,2,3

Note:

1. Typical value at  $T_A = 25^\circ C$ .
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Without CLK toggling.
4. 0.5x Refresh
5. Full Array Refresh

**Table 32. DC Characteristics-3.3V**

Symbol	Parameter	Min	Typ	Max	Unit	Note
V <sub>DD</sub>	Supply Voltage	2.7		3.6	V	
V <sub>DDQ</sub>	I/O Supply Voltage	2.7		3.6	V	
V <sub>IH</sub>	Input high voltage	V <sub>DDQ</sub> – 0.4		V <sub>DDQ</sub> + 0.2	V	
V <sub>IL</sub>	Input low voltage	-0.2		0.4	V	
V <sub>OH</sub>	Output high voltage (I <sub>OH</sub> =-0.2mA)	0.8 V <sub>DDQ</sub>			V	
V <sub>OL</sub>	Output low voltage (I <sub>OL</sub> =+0.2mA)			0.2 V <sub>DDQ</sub>	V	
I <sub>LI</sub>	Input Pin leakage current	-1		1	μA	
I <sub>LO</sub>	Output Pin leakage current	-1		1	μA	
I <sub>DD</sub>	Read @166MHz		17	19	mA	1,2
	Read @200MHz		20	22	mA	1,2
I <sub>DD</sub>	Write @166MHz		16	18	mA	1,2
	Write @200MHz		18	20	mA	1,2
I <sub>SB</sub>	Standby current (-40 to 85°C)		100	250	μA	1,2,3,4,5
I <sub>DPD</sub>	Deep Power Down current		7	13	μA	1,2,3
I <sub>RST</sub>	Software Reset current		100	350	μA	1,2,3

Note:

1. Typical value at T<sub>A</sub> = 25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Without CLK toggling.
4. 0.5x Refresh
5. Full Array Refresh

## 6.7 ISB and ILPM Partial Array Refresh Current-1.8V

**Table 33. Typical-mean PASR Current @ 25°C**

PASR	I <sub>SB</sub> -typical mean	I <sub>LPM</sub> -typical mean	Unit
Full	66	20	μA
1/2	60	14	μA
1/4	57	11	μA
1/8	55	10	μA

**Table 34. Typical-mean PASR Current @ 85°C**

PASR	I <sub>SB</sub> -typical mean	I <sub>LPM</sub> -typical mean	Unit
Full	200	120	μA
1/2	150	72	μA
1/4	125	48	μA
1/8	110	24	μA

Note:

1. Current at 25°C is only attainable by enabling 0.5x Refresh Frequency.
2. PASR Current is only characterized without CLK toggling.
3. I<sub>LPM</sub> current is only guaranteed after 150ms into Low Power Mode.

## 6.8 ISB and ILPM Partial Array Refresh Current-3.3V

**Table 35. Typical-mean PASR Current @ 25°C**

PASR	I <sub>SB</sub> -typical mean	I <sub>LPM</sub> -typical mean	Unit
Full	100	40	μA
1/2	95	34	μA
1/4	90	31	μA
1/8	85	30	μA

**Table 36. Typical-mean PASR Current @ 85°C**

PASR	I <sub>SB</sub> -typical mean	I <sub>LPM</sub> -typical mean	Unit
Full	210	160	μA
1/2	185	112	μA
1/4	170	98	μA
1/8	160	64	μA

Note:

1. Current at 25°C is only attainable by enabling 0.5x Refresh Frequency.
2. PASR current is only characterized without CLK toggling.
3. I<sub>LPM</sub> current is only guaranteed after 150ms into Low Power Mode.

## 6.9 AC Characteristics

**Table 37. AC parameters**

Symbol	Parameter	Min	Max	Unit
tCLK	CLK period (166MHz)	6		ns
	CLK period (200MHz)	5		ns
	CLK period (266MHz)	3.75		ns
	CLK period (333MHz)	3		ns
	CLK period (400MHz)	2.5		ns
tCH/tCL	CLK high/low width	0.45	0.55	tCLK
tCPH	CS# HIGH between subsequent burst operations (166MHz)	18		ns
	CS# HIGH between subsequent burst operations (200MHz)	24		ns
	CS# HIGH between subsequent burst operations (266MHz)	27		ns
	CS# HIGH between subsequent burst operations (333MHz)	29		ns
	CS# HIGH between subsequent burst operations (400MHz)	32		ns
tCSM	CS# low pulse width (-40°C to 85°C)		4	μs
	CS# low pulse width (-40°C to 105°C)		1	μs
	CS# low pulse width (minimum = 3 clock)	3		tCLK
tCSP	CS# setup time to CLK rising edge (166/200MHz)	2		ns
	CS# setup time to CLK rising edge (266MHz)	1.8		ns
	CS# setup time to CLK rising edge (333/400MHz)	1.5		ns
tCHD	CS# hold time from CLK falling edge (166/200MHz)	2		ns
	CS# hold time from CLK falling edge (266MHz)	1.8		ns
	CS# hold time from CLK falling edge (333/400MHz)	1.5		ns

Symbol	Parameter	Min	Max	Unit
tSP	Setup time to active CLK edge (166MHz)	0.6		ns
	Setup time to active CLK edge (200MHz)	0.5		ns
	Setup time to active CLK edge (266/333/400MHz)	0.4		ns
tHD	Hold time from active CLK edge (166MHz)	0.6		ns
	Hold time from active CLK edge (200MHz)	0.5		ns
	Hold time from active CLK edge (266/333/400MHz)	0.4		ns
tHZ	Chip disable to DQ/DQS output high-Z	5		ns
tDSV (1.8V)	Data Strobe Valid (166MHz)		12	ns
	Data Strobe Valid (200/266/333/400MHz)		5	ns
tDSV (3.3V)	Data Strobe Valid (166MHz)		12	ns
	Data Strobe Valid (200MHz)		6.5	ns
tRBXwait	Row boundary crossing wait time	30	65	ns
tRC	Write Cycle	60		ns
	Read Cycle	60		ns
tRFC	Refresh cycle time with manual refresh enabled	45		ns
tREFW	Refresh window (-40°C to 85°C)	4		ms
	Refresh window (-40°C to 105°C)	1		ms
tLPI	Minimum low power mode duration	100		µs
tXLP	Low power mode exit CS# low to CLK setup time	100		µs
tXPLP	Low power mode exit CS# low pulse width	60	500	ns
tDPD	Minimum deep power down duration	500		µs
tDPDp	Minimum period between DPD	500		µs
tXDPD	DPD exit CS# low to CLK setup time	150		µs
tXPDPD	DPD exit CS# low to CLK pulse width	60		ns
tPU	Device initialization	150		µs
tRP	RESET# low pulse width	1000		ns
tRST	Reset to command valid	2000		ns
tCQLZ	CLK rising edge to DQS low	1	6	ns
tDQSCK	DQS output access time from CLK	1	5	ns
tDQSQ	DQS-DQ skew (166MHz)	-0.5	0.5	ns
	DQS-DQ skew (200MHz)	-0.4	0.4	ns
	DQS-DQ skew (266/333/400MHz)	-0.3	0.3	ns
tDS	DQ and DM input setup time (166MHz)	0.6		ns
	DQ and DM input setup time (200MHz)	0.5		ns
	DQ and DM input setup time (266/333/400MHz)	0.4		ns
tDH	DQ and DM input hold time (166MHz)	0.6		ns
	DQ and DM input hold time (200MHz)	0.5		ns
	DQ and DM input hold time (266/333/400MHz)	0.4		ns



## 7 Revision History

Version No	Description	Page	Date
1.0	Initial release	---	2025/4/21

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