GDB4CBQN

DATASHEET

Features

- Device configuration:
  16Gb: (2 x 8Gb) LPDDR4/4x SDRAM
- Ultra-low-voltage core and I/O power supply
  VDD1=1.70~1.95V; 1.80V nominal
  VDD2=1.06~1.17V; 1.10V nominal
  VDDQ=1.06~1.17V; 1.10V nominal
  or Low VDDQ=0.57~0.65V; 0.60V nominal
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL=16,32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Programmable VSS (ODT) termination

Address Table

Die Configuration	**512Mbx16**
Bank Address	BA0~BA2
Row Address	A0~A15
Column Address	A0~A9

Ordering Information

Part Number Decoding

G D B 4 C B Q N - M x

Speed Type
J: 3200Mbps
K: 3733Mbps
L: 4266Mbps

Operating Temp.
M: Mobile Temp. (-25℃~85 ℃)

Product Version
N: 1st version (special)

Voltage
Q: VDD1/VDD2/VDDQ: 1.8V/1.1V/1.1V&0.6V

Bit Organization
B: x32 2CH, 1CS, DDP

Package Type
C: 200-Ball FBGA

Density
4: 16Gb

Product Type
B: LPDDR4x

Product Family
D: DRAM

Company
G: Global XC Memory

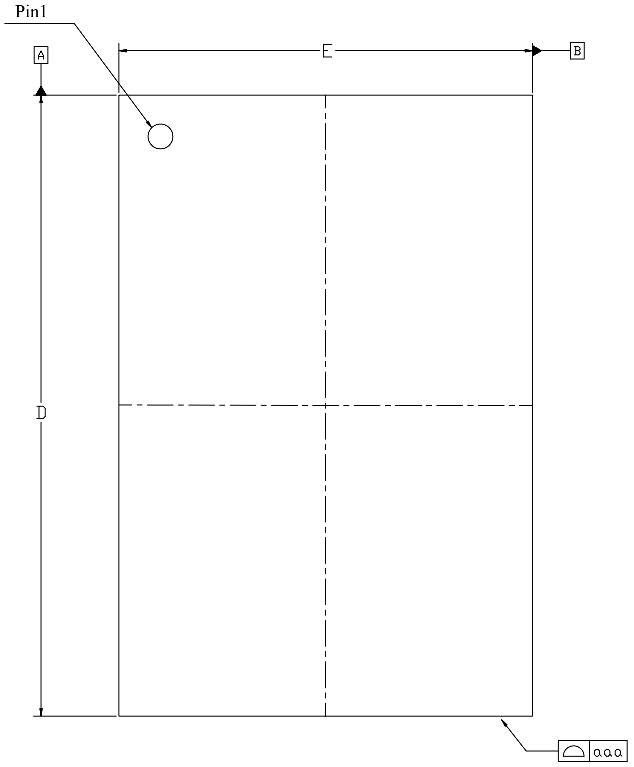
Valid Part Numbers

Part Number	Density	Organization	Data Rate	Package
GDB4CBQN-MJ	16Gb	2CHx32	3200Mbps	200-Ball FBGA
GDB4CBQN-MK	16Gb	2CHx32	3733Mbps	200-Ball FBGA
GDB4CBQN-ML	16Gb	2CHx32	4266Mbps	200-Ball FBGA

Contents

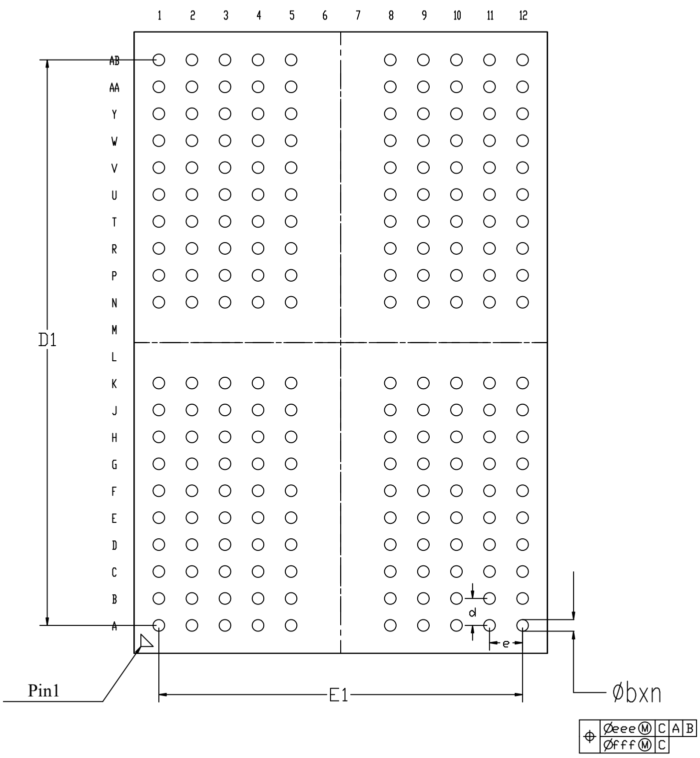
1 Package Information

1.1 Package 200-Ball FBGA (x32)

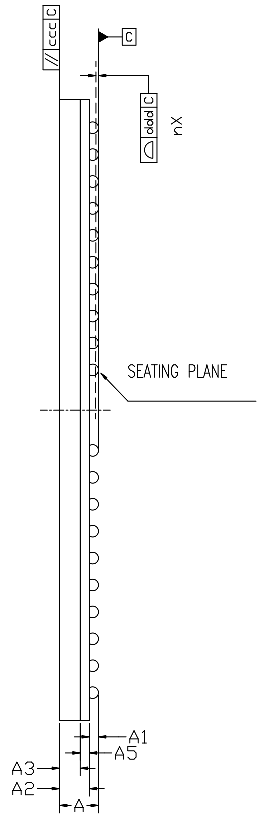


TOP VIEW

	Symbol	Dimension in mm		
		Min	Normal	Max
TOTAL THICKNESS	A	0.670	0.770	0.870
STAND OFF	A1	0.170	0.220	0.270
SBT+MOLD THICKNESS	A2	0.510	0.550	0.590
MOLD THICKNESS	A3	0.405	0.420	0.435
SUBSTRATE THICKNESS	A5	0.117	0.130	0.143
BALL WIDTH	Φb	0.260	0.310	0.360
BALL PITCH	d	0.650 BASIC		
	e	0.800 BASIC		
BALL COUNT	n	200		
BODY SIZE	D	14.900	15.000	15.100
	E	9.900	10.000	10.100
EDGE BALL CENTER TO CENTER	D1	13.550	13.650	13.750
	E1	8.700	8.800	8.900
PKG EDGE TOLERANCE	aaa	0.100		
MOLD FLATNESS	ccc	0.100		
COPLANARITY	ddd	0.100		
BALL OFFSET(PACKAGE)	eee	0.150		
BALL OFFSET(BALL)	fff	0.080		
JEDEC		MO-311(REF)		



BOTTOM VIEW



SIDE VIEW

2 Ball Assignments

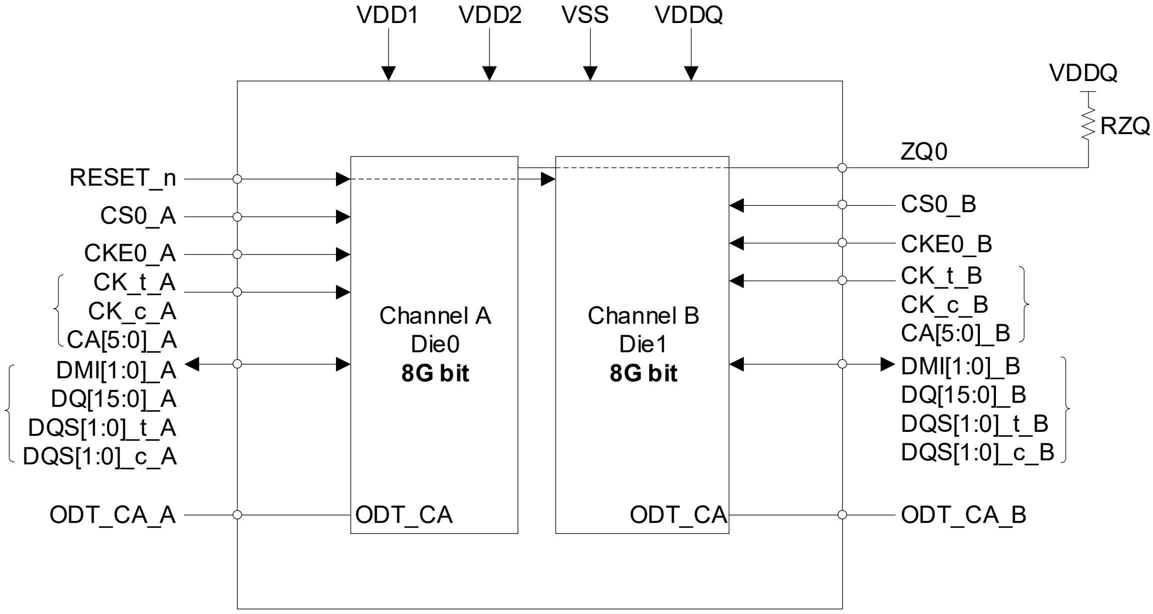
2.1 200-Ball FBGA (x32) Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

Note:

1. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows using MO-311 0.80mm pitch.
2. Top View, A1 in top left corner. CS1_A/B, CKE1_A/B, ZQ1 are floating for 2GB package.
3. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
4. ZQ2, CKE2_A, CKE2_B, CS2_A and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.
5. Die pad VSS and VSSQ signals are combined to VSS package balls.
6. Package requires dual channel die or functional equivalent of single channel die-stack.

2.2 Block Diagram



2.3 Ball Description

“_A” and “_B” indicate DRAM channels. “_A” pads are present in all devices while “_B” pads are present in dual channel SDRAM devices only.

LPDDR4x pad definitions are the same as LPDDR4, except ODT_CA pins as described in the table below.

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A&B) has its own clock pair.
CKE_A, CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A&B) has its own CKE signal.
CS_A, CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A&B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data Input/Output:** Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A&B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A&B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

ODT_CA_A, ODT_CA_B	Input	**CA ODT Control:** **LPDDR4:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. **LPDDR4x:** The ODT_CA pin is ignored by LPDDR4x devices. ODT_CS/CA/CK Function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS.

3 Simplified LPDDR4 State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

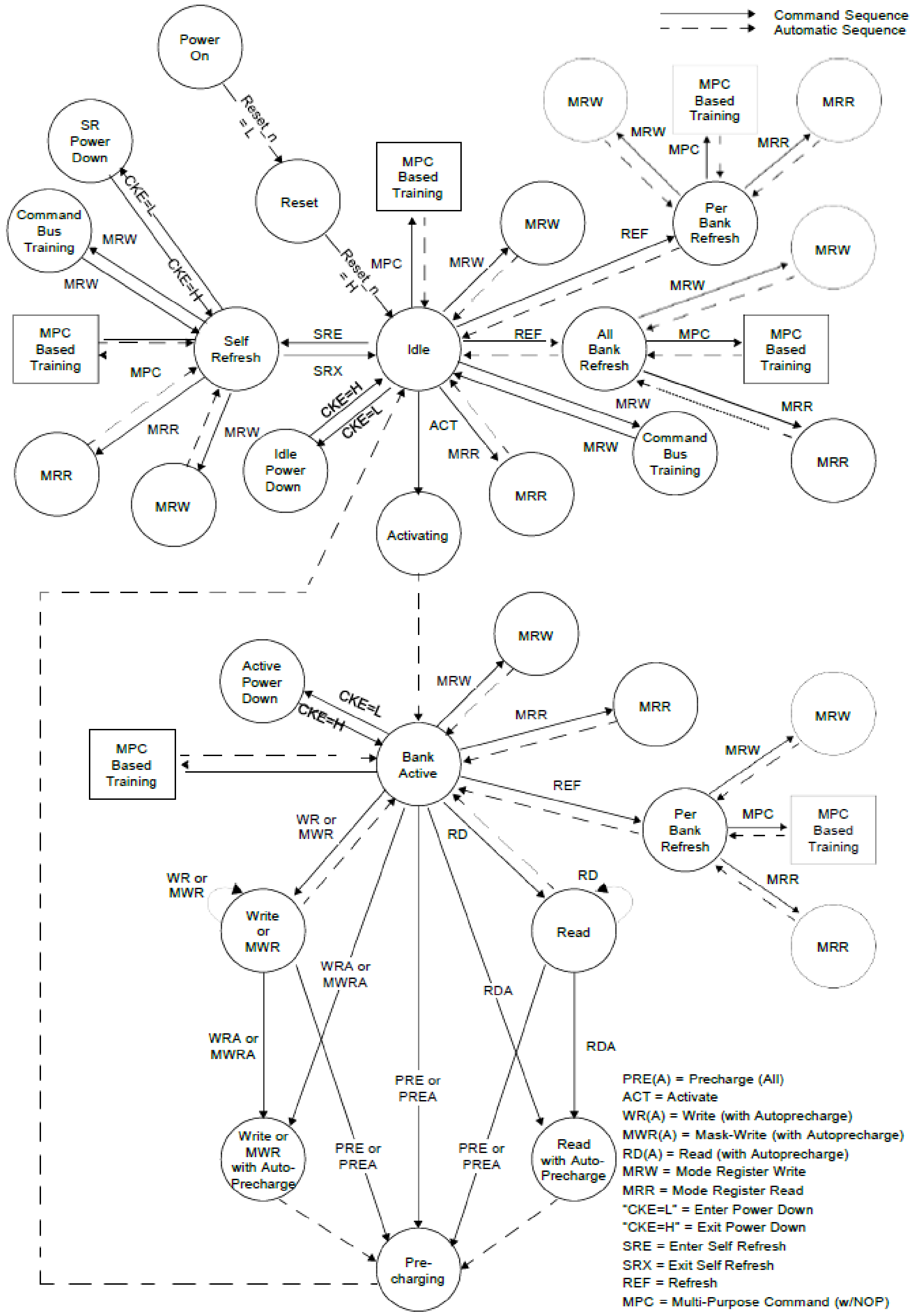


Figure 3-1 Simplified State Diagram

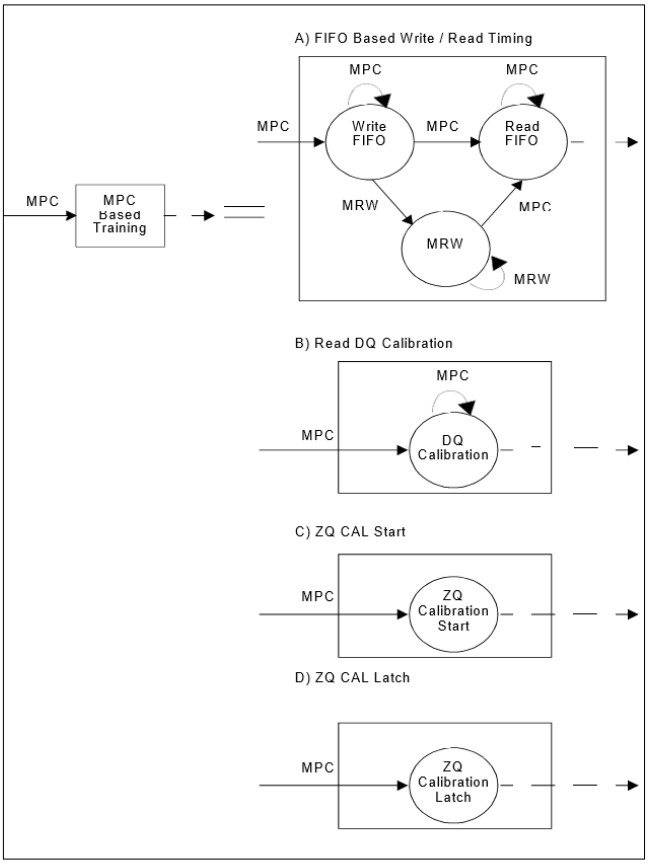


Figure 3-2 Simplified State Diagram

Note:

1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

4 Mode Registers

4.1 Mode Register Default Settings

Table 4-1 MRS defaults settings

Item	Mode Register Setting	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00b	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0b	WRITE latency set 0 is selected
WL	MR2 OP[5:3]	000b	WL = 4
RL	MR2 OP[2:0]	000b	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000b	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00b	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000b	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000b	DQ ODT is disabled
VREF(CA) Setting	MR12 OP[6]	1b	VREF(CA) Range[1] enabled
VREF(CA) Value	MR12 OP[5:0]	001101b	Range1 : 27.2% of VDD2
VREF(DQ) Setting	MR14 OP[6]	1b	VREF(DQ) Range[1] enabled
VREF(DQ) Value	MR14 OP[5:0]	001101b	Range1 : 27.2% of VDDQ

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

4.2 Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 4-2 Mode Register Assignments

<table>
<tr><th>MR#</th><th>MA[7:0]</th><th>Access</th><th>OP7</th><th>OP6</th><th>OP5</th><th>OP4</th><th>OP3</th><th>OP2</th><th>OP1</th><th>OP0</th></tr>
<tr><td>0</td><td>00h</td><td>R</td><td>CATR</td><td>RFU</td><td>RFU</td><td colspan="2">RZQI</td><td>RFU</td><td>RFU</td><td>REF</td></tr>
<tr><td>1</td><td>01h</td><td>W</td><td>RPST</td><td colspan="3">nWR (for AP)</td><td>RD-PRE</td><td>WR-PRE</td><td colspan="2">BL</td></tr>
<tr><td>2</td><td>02h</td><td>W</td><td>WR Lev</td><td>WLS</td><td colspan="3">WL</td><td colspan="3">RL</td></tr>
<tr><td>3</td><td>03h</td><td>W</td><td>DBI-WR</td><td>DBI-RD</td><td colspan="3">PDDS</td><td>PPRP</td><td>WR PST</td><td>PU-CAL</td></tr>
<tr><td>4</td><td>04h</td><td>R/W</td><td>TUF</td><td colspan="2">Thermal Offset</td><td>PPRE</td><td>SR Abort</td><td colspan="3">Refresh Rate</td></tr>
<tr><td>5</td><td>05h</td><td>R</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6</td><td>06h</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>07h</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>8</td><td>08h</td><td>R</td><td colspan="2">IO Width</td><td colspan="4">Density</td><td colspan="2">Type</td></tr>
</table>

MR#	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
9	09h	W	Vendor Specific Test Register							
10	0Ah	W	RFU							ZQ-Reset
11	0Bh	W	RFU	CA ODT			RFU	DQ ODT		
12	0Ch	R/W	RFU	VR-CA	VREF(CA)					
13	0Dh	W	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	0Eh	R/W	RFU	VR-DQ	VREF(DQ)					
15	0Fh	W	Lower-Byte Invert Register for DQ Calibration							
16	10h	W	PASR Bank Mask							
17	11h	W	PASR Segment Mask							
18	12h	R	DQS Oscillator Count - LSB							
19	13h	R	DQS Oscillator Count - MSB							
20	14h	W	Upper-Byte Invert Register for DQ Calibration							
21	15h	W	RFU							
22	16h	W	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		
23	17h	W	DQS interval timer run time setting							
24	18h	R/W	TRR mode	TRR mode BAn			Unltd MAC	MAC value		
25	19h	R	PPR Resource							
26-31	1Ah~1Fh	-	RFU							
32	20h	W	DQ Calibration Pattern “A” (default = 5Ah)							
33-39	21~27h	-	RFU							
40	28h	W	DQ Calibration Pattern “B” (default = 3Ch)							

Note:

1. RFU bits must be set to 0 during MRW commands.
2. RFU bits are read as 0 during MRR commands.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
4. RFU mode registers must not be written.
5. Writes to read-only registers will not affect the functionality of the device.

5 Absolute Maximum Ratings

This chapter specifies absolute maximum DC ratings. Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5-1 Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.4		1
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.4		1
Voltage on any ball except VDD1 relative to VSS	VIN, VOUT	-0.4	1.4		-
Storage Temperature	T_{STG}	-55	125	°C	2

Note:

1. See “Power-Ramp” for relationships between power supplies.
2. Storage temperature is the case surface temperature on the center/top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2.

6 AC and DC Operating Conditions

6.1 Recommended DC Operating Conditions for Low Voltage

Table 6-1 LPDDR4 Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer Power	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	1.06	1.1	1.17	V	2,3

Note:

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45mV (peak-peak) from DC to 20MHz.

Table 6-2 LPDDR4x Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Note
Core 1 Power	VDD1	1.7	1.8	1.95	V	1,2
Core 1 Power/Input Buffer Power	VDD2	1.06	1.1	1.17	V	1,2,3
I/O Buffer Power	VDDQ	0.57	0.6	0.65	V	2,3,4,5

Note:

1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20MHz exceeding a peak-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.
4. VDDQ(max) may be extended to 0.67V as an option in case the operating clock frequency is equal or less than 800MHz.
5. Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57V~0.65V).

6.2 Input Leakage Current

Table 6-3 Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input Leakage current	I_L	-4	4	uA	1,2

Note:

1. For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V≤VIN≤VDD2 (All other pins not under test=0V).
2. CA ODT is disabled for CK_t, CK_c, CS and CA.

6.3 Input/Output Leakage Current

Table 6-4 Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/Output Leakage current	I_{OZ}	-5	5	uA	1,2

Note:

1. For DQ, DQS_t, DQS_c and DMI. Any I/O 0V⩽VOUT⩽VDDQ.
2. I/Os status are disabled: High Impedance and ODT Off.

6.4 DRAM Component Operating Temperature Range

Table 6-5 Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit	Note
Standard	T_{OPER}	-25	85	°C	-
Elevated		85	105	°C	-

Note:

1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.
2. Some applications require operation of LPDDR4 in the maximum temperature conditions in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. See MR4.
3. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Elevated Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

7 AC and DC Input Measurement Levels

7.1 1.1V High Speed LVCMOS (HS_LLVCMOS)

7.1.1 Standard Specifications

All voltages are referenced to ground except where noted.

7.1.2 DC Electrical Characteristics

7.1.2.1 Input Level for CKE

This definition applies to CKE_A/CKE_B.

Table 7-1 Input Level for CKE

Parameter	Symbol	Min	Max	Unit	Note
Input high level (AC)	VIH(AC)	0.75*VDD2	VDD2+0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25*VDD2	V	1
Input high level (DC)	VIH(DC)	0.65*VDD2	VDD2+0.2	V	-
Input low level (DC)	VIL(DC)	-0.2	0.35*VDD2	V	-

Note:

1. Refer AC Overshoot and Undershoot for VIH(AC) and VIL(AC).

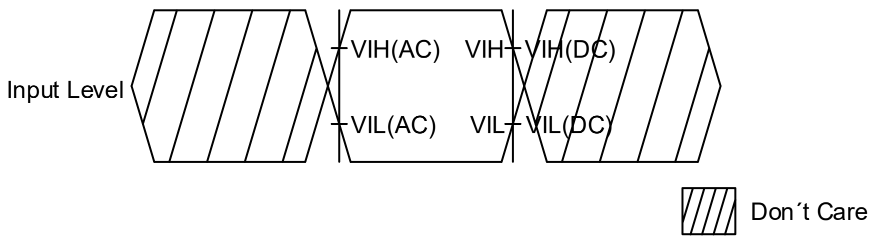


Figure 7-1 Input AC Timing Definition for CKE

Note:

1. AC level is guaranteed transition point.
2. DC level is hysteresis.

7.1.2.2 Input Level for RESET_n and ODT_CA

This definition applies to RESET_n and ODT_CA.

Table 7-2 Input Level for RESET_n and ODT_CA

Parameter	Symbol	Min	Max	Unit	Note
Input high level	VIH	0.80*VDD2	VDD2+0.2	V	1
Input low level	VIL	-0.2	0.2*VDD2	V	1

Note:

1. Refer AC Overshoot and Undershoot for VIH and VIL.

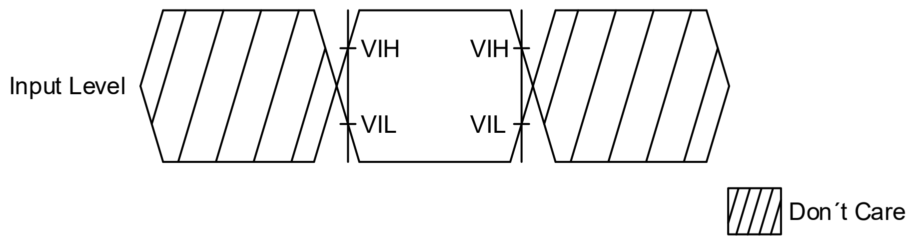


Figure 7-2 Input AC Timing Definition for RESET_n and ODT_CA

7.1.3 AC Overshoot and Undershoot

Table 7-3 AC Over/Undershoot for Address and Control Pins

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35V
Maximum peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD/VDDQ	0.8V-ns
Maximum undershoot area below VSS/VSSQ	0.8V-ns

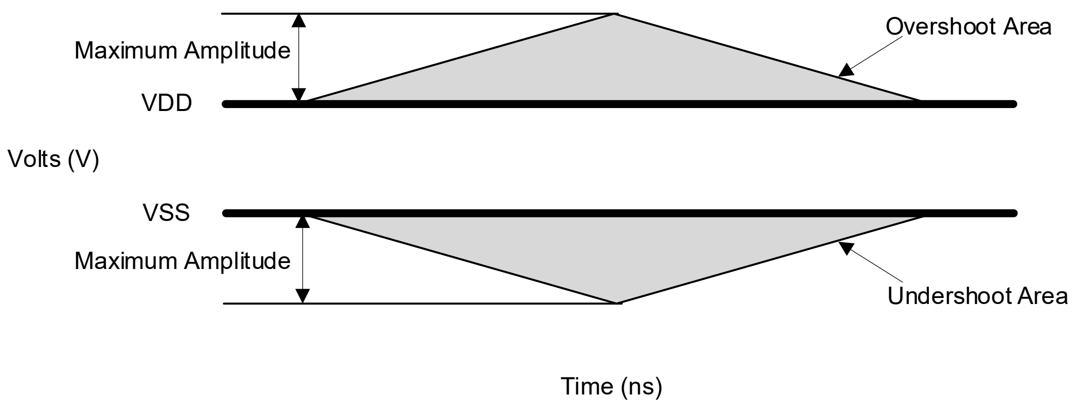


Figure 7-3 AC Overshoot and Undershoot Definition for Address and Control Pins

7.2 Differential Input Voltage

7.2.1 Differential Input Voltage for Clock

The minimum input voltage need to satisfy both VIN.DIFF_CK and VIN.DIFF_CK/2 specification at input receiver and their measurement period is 1tCK. VIN.DIFF_CK is the peak-peak voltage centered on 0 volts differential and VIN.DIFF_CK/2 is max and min peak voltage from 0V.

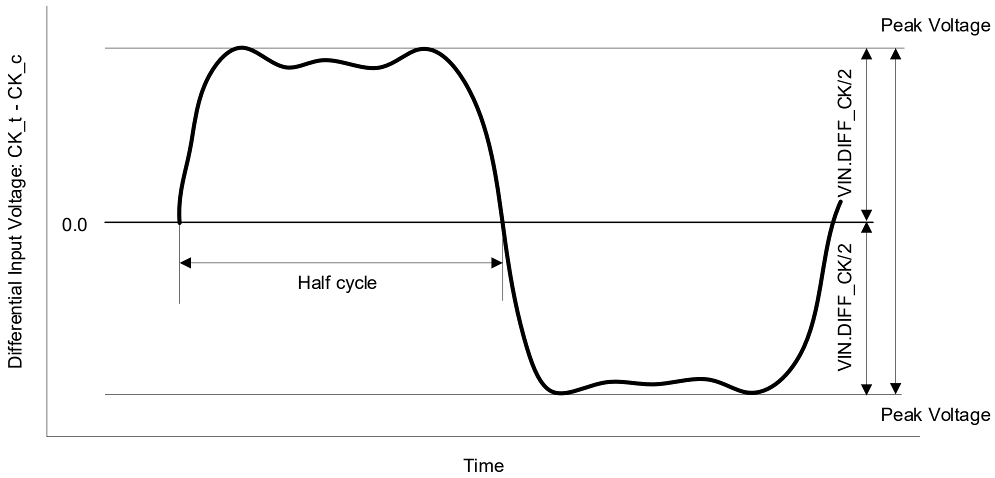


Figure 7-4 CK Differential Input Voltage

Table 7-4 CK Differential Input Voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	VIN.DIFF_CK	420	-	380	-	360	-	mV	1,2

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. The peak voltage of Differential CK signals is calculated in a following equation.
   - VIN.DIFF_CK=(Max Peak Voltage)-(Min Peak Voltage)
   - Max Peak Voltage=Max(f(t))
   - Min Peak Voltage=Min(f(t))
   - f(t)=VCK_t-VCK_c

7.2.2 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in a following equation.

VIH.DIFF.Peak Voltage=Max(f(t))

VIL.DIFF.Peak Voltage=Min(f(t))

f(t)=VCK_t-VCK_c

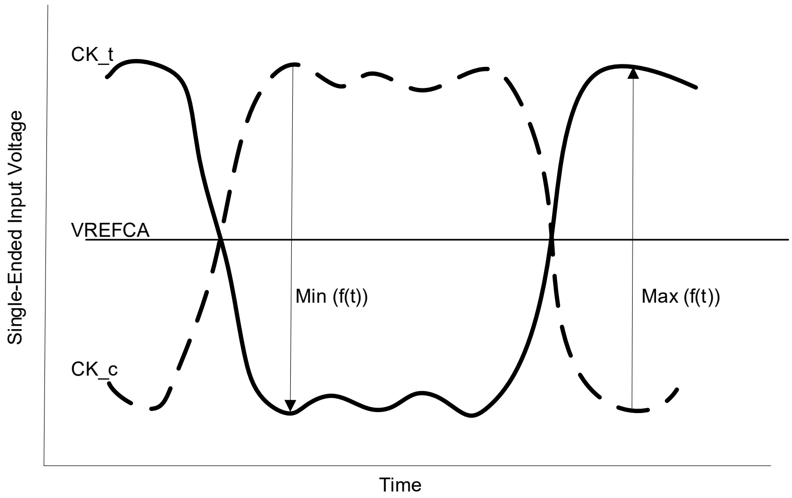


Figure 7-5 Definition of Differential Clock Peak Voltage

Note:

1. VREFCA is LPDDR4x SDRAM internal setting value by VREF Training.

7.2.3 Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy both VIN.SE_CK, VIN.SE_CK_HIGH/LOW specification at input receiver.

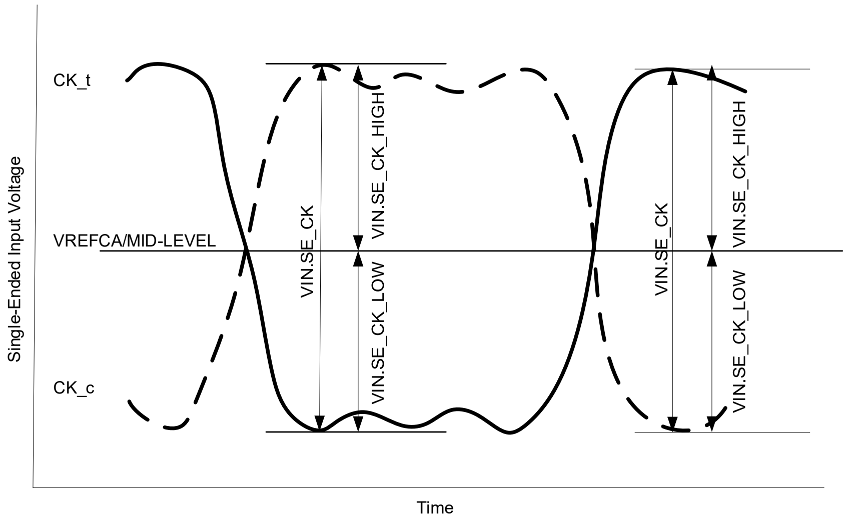


Figure 7-6 Clock Single-Ended Input Voltage

Note:

1. VREFCA is LPDDR4x SDRAM internal setting value by VREF Training.

Table 7-5 Clock Single-Ended Input Voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock single-ended input voltage	VIN.SE_CK	210	-	190	-	180	-	mV	1
Clock single-ended input voltage HIGH from VREFDQ	VIN.SE_CK_HIGH	105	-	95	-	90	-	mV	1
Clock single-ended input voltage LOW from VREFDQ	VIN.SE_CK_LOW	105	-	95	-	90	-	mV	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

7.2.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 7-7 and the following Tables.

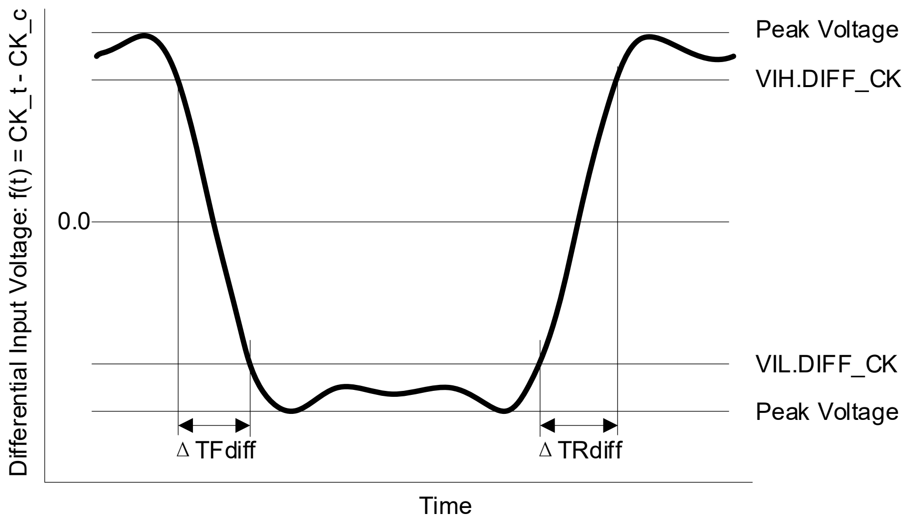


Figure 7-7 Differential Input Slew Rate Definition for CK_t, CK_c

Note:

1. Differential signal rising edge from VIL.DIFF_CK to VIH.DIFF_CK must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF_CK to VIL.DIFF_CK must be monotonic slope.

Table 7-6 Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge(CK_t-CK_c)	VIL.DIFF_CK	VIH.DIFF_CK	|VIL.DIFF_CK-VIH.DIFF_CK|/ΔTRdiff
Differential input slew rate for falling edge(CK_t-CK_c)	VIH.DIFF_CK	VIL.DIFF_CK	|VIL.DIFF_CK-VIH.DIFF_CK|/ΔTFdiff

Table 7-7 Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input HIGH	VIH.DIFF_CK	175	-	155	-	145	-	mV	1
Differential Input LOW	VIL.DIFF_CK	-	-175	-	-155	-	-145	mV	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

Table 7-8 Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	V/ns	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

7.2.5 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 7-9. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the MID-LEVEL that is VREFCA.

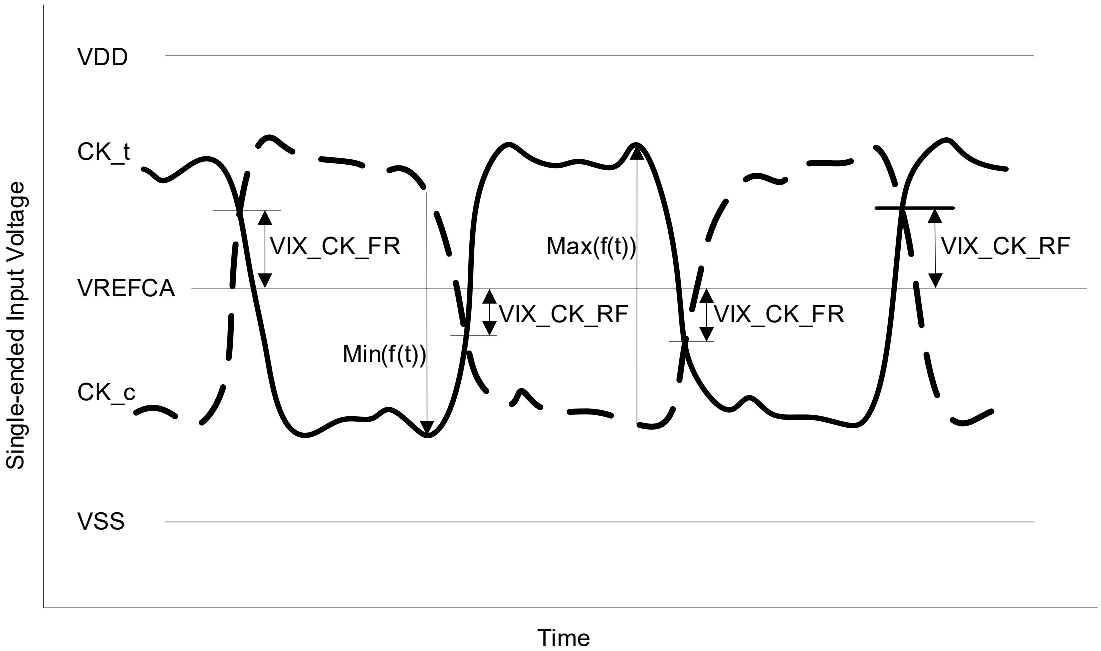


Figure 7-8 VIX Definition (Clock)

Note:

1. The base level of VIX_CK_FR/RF is VREFCA that is LPDDR4x SDRAM internal setting value by VREF Training.

Table 7-9 Cross Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Differential input cross point voltage ratio	VIX_CK_ratio	-	25	-	25	-	25	%	1,2,3,4,5

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. VIX_CK_ratio is defined by this equation: VIX_CK_ratio=VIX_CK_FR/|Min(f(t))|.
3. VIX_CK_ratio is defined by this equation: VIX_CK_ratio=VIX_CK_RF/Max(f(t)).
4. VIX_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
5. VIX_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
6. In LPDDR4x un-terminated case, CK MID-LEVEL is calculated as:
   HIGH LEVEL=VDDQ, LOW LEVEL=VSS, MID-LEVEL=VDDQ/2.
7. In LPDDR4 un-terminated case, MID-LEVEL must be equal or lower than 369mV (33.6% of VDD2).

7.2.6 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both VIN.DIFF_DQS and VIN.DIFF_DQS/2 specification at input receiver and their measurement period is 1UI(tCK/2). VIN.DIFF_DQS is the peak-peak voltage centered on 0 volts differential and VIN.DIFF_DQS/2 is Max and Min peak voltage from 0V.

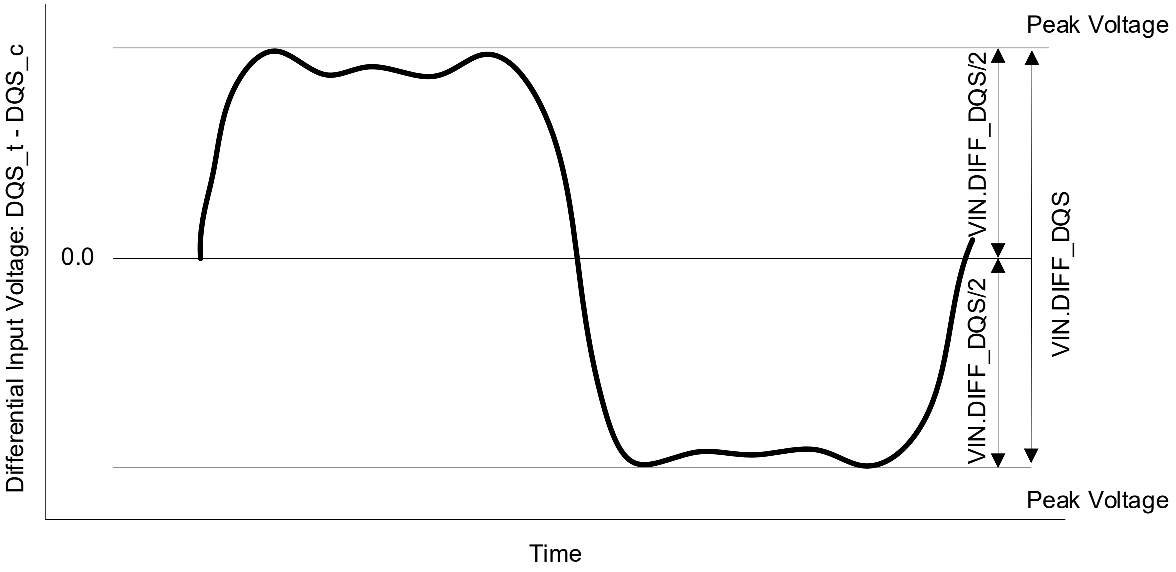


Figure 7-9 DQS Differential Input Voltage

Table 7-10 DQS Differential Input Voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS differential input	VIN.DIFF_DQS	360	-	360	-	340	-	mV	1,2

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. The peak voltage of Differential DQS signals is calculated in a following equation.
   - VIN.DIFF_DQS=(Max Peak Voltage)-(Min Peak Voltage)
   - Max Peak Voltage=Max(f(t))
   - Min Peak Voltage=Min(f(t))
   - f(t)=VDQS_t-VDQS_c

7.2.7 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated in a following equation.

- VIH.DIFF.Peak Voltage=Max(f(t))
- VIL.DIFF.Peak Voltage=Min(f(t))
- f(t)=VDQS_t-VDQS_c

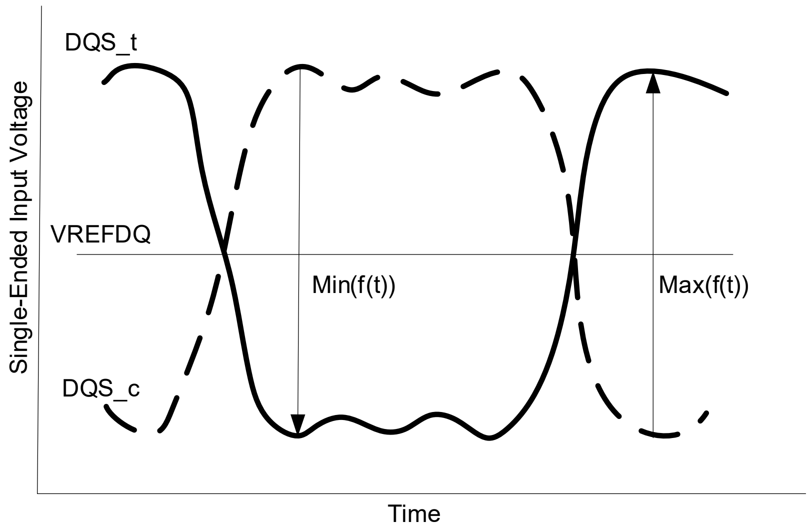


Figure 7-10 Definition of Differential DQS Peak Voltage

Note:

1. VREFDQ is LPDDR4x SDRAM internal setting value by VREF Training.

7.2.8 Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both VIN.SE_DQS, VIN.SE_DQS_HIGH/LOW specification at input receiver.

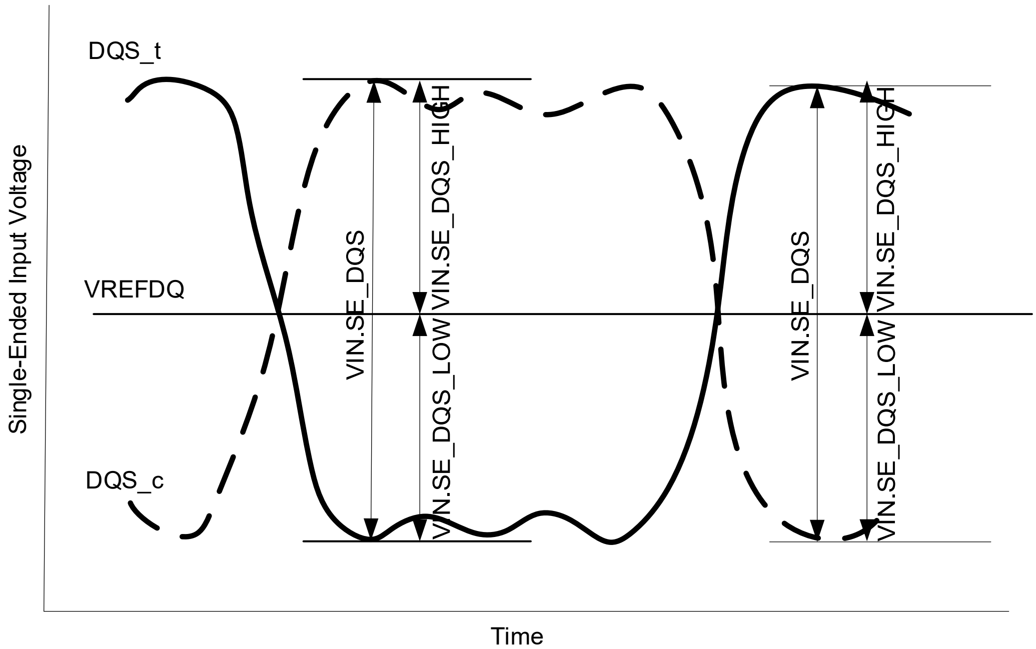


Figure 7-11 **DQS Single-Ended Input Voltage**

Note:

1. VREFDQ is LPDDR4x SDRAM internal setting value by VREF Training.

Table 7-11 DQS Single-Ended Input Voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS single-ended input voltage	VIN.DIFF_DQS	180	-	180	-	170	-	mV	1
DQS single-ended input voltage HIGH from VREFDQ	VIN.SE_DQS_HIGH	90	-	90	-	85	-	mV	1
DQS single-ended input voltage LOW from VREFDQ	VIN.SE_DQS_LOW	90	-	90	-	85	-	mV	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

7.2.9 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 7-12 and Table 7-12.

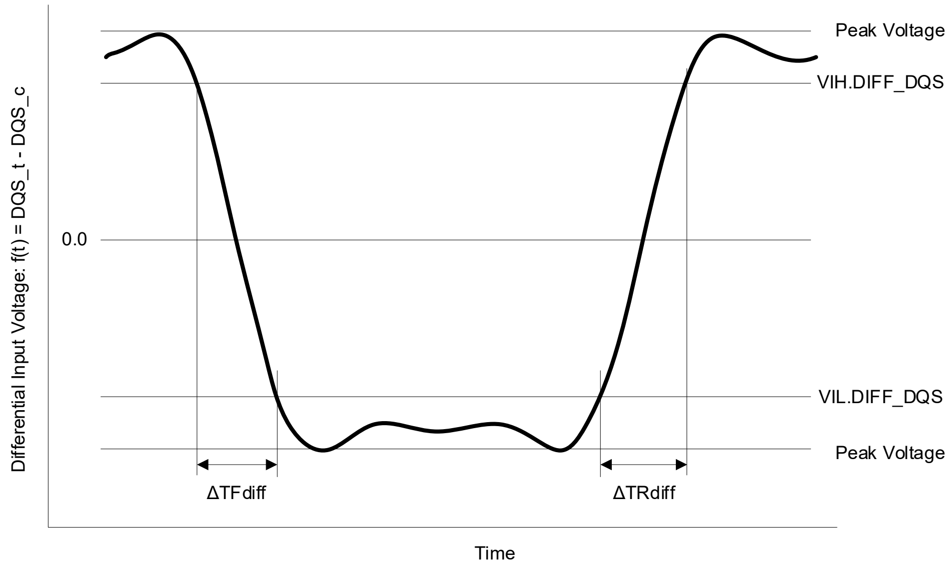


Figure 7-12 Differential Input Slew Rate Definition for DQS_t, DQS_c

Note:

1. Differential signal rising edge from VIL.DIFF_DQS to VIH.DIFF_DQS must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF_DQS to VIL.DIFF_DQS must be monotonic slope.

Table 7-12 Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t-DQS_c)	VIL.DIFF_DQS	VIH.DIFF_DQS	|VIL.DIFF_DQS-VIH.DIFF_DQS|/ΔTRdiff
Differential input slew rate for falling edge (DQS_t-DQS_c)	VIH.DIFF_DQS	VIL.DIFF_DQS	|VIL.DIFF_DQS-VIH.DIFF_DQS|/ΔTFdiff

Table 7-13 Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input HIGH	VIH.DIFF_DQS	140	-	140	-	120	-	mV	1
Differential Input LOW	VIL.DIFF_DQS	-	-140	-	-140	-	-120	mV	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

Table 7-14 Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate	SRIdiff	2	14	2	14	2	14	V/ns	1

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

7.2.10 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 7-15.

The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the MID-LEVEL that is VREFDQ.

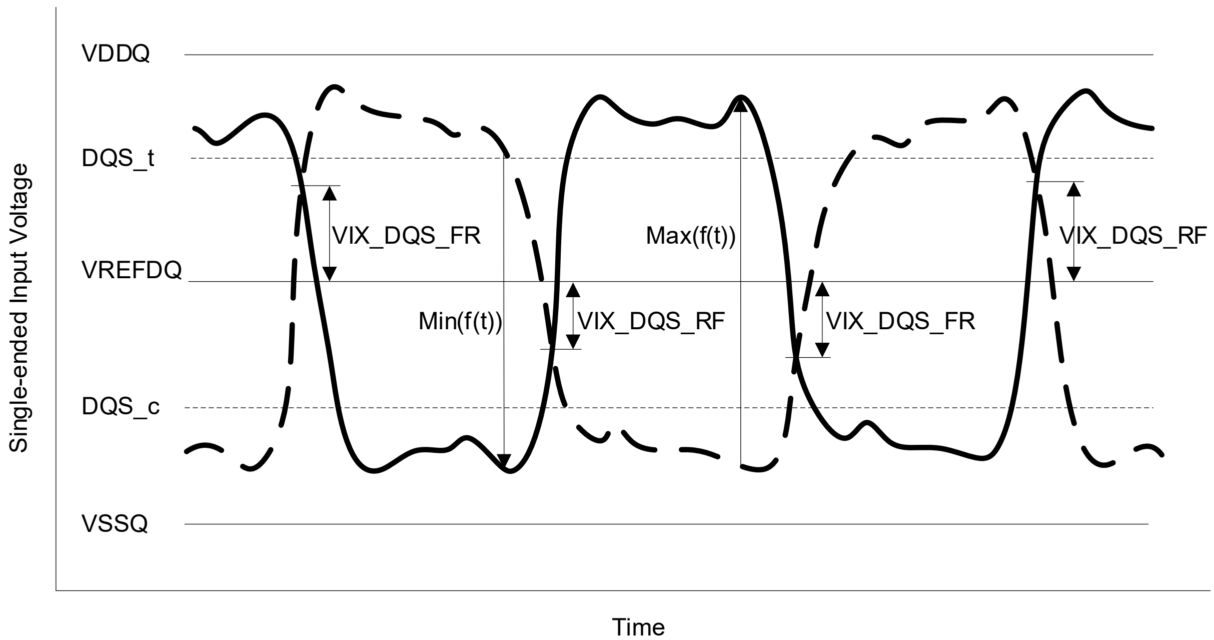


Figure 7-13 VIX Definition (DQS)

Note:

1. The base level of VIX_DQS_FR/RF is VREFDQ that is LPDDR4x SDRAM internal setting value by VREF Training.

Table 7-15 Cross Point Voltage for Differential Input Signals (DQS)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS Differential input cross point voltage ratio	VIX_DQS_Ratio	-	20	-	20	-	20	%	1,2,3

Note:

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. VIX_DQS_ratio is defined by this equation: VIX_DQS_ratio=VIX_DQS_FR/|Min(f(t))|.
3. VIX_DQS_ratio is defined by this equation: VIX_DQS_ratio=VIX_DQS_RF/Max(f(t)).

7.3 AC/DC Input level for ODT Input

Table 7-16 Input Level for ODT

Parameter	Symbol	Min	Max	Unit	Note
ODT Input high level (AC)	VIHODT(AC)	0.75*VDD	VDD+0.2	V	1
ODT Input low level (AC)	VILODT(AC)	-0.2	0.25*VDD	V	1
ODT Input high level (DC)	VIHODT(DC)	0.65*VDD	VDD+0.2	V	-
ODT Input low level (DC)	VILODT(DC)	-0.2	0.35*VDD	V	-

Note:

1. See Overshoot and Undershoot Specifications.

8 AC And DC Output Measurement Levels

8.1 Single-Ended Output Slew Rate

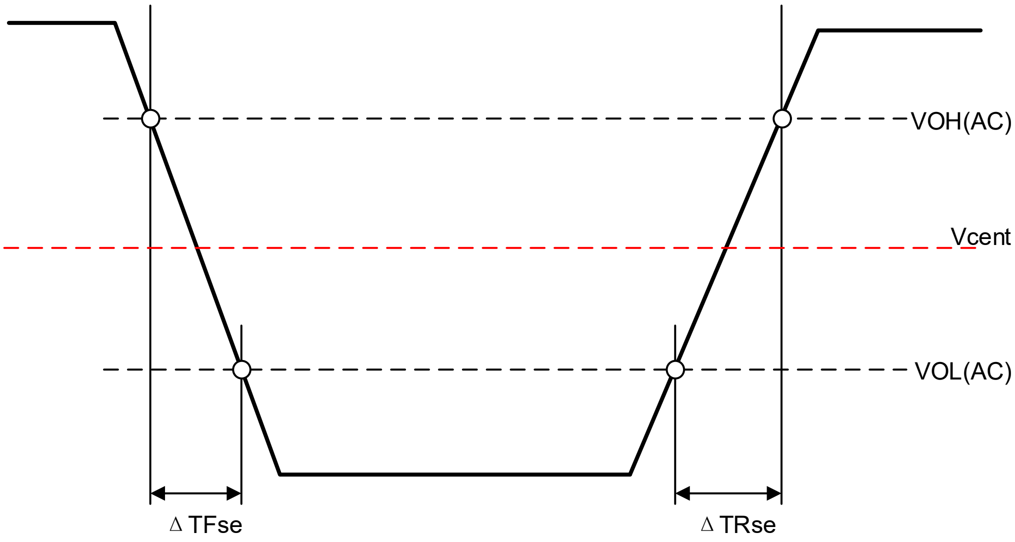


Figure 8-1 Single-Ended Output Slew Rate Definition

Table 8-1 LPDDR4 Output Slew Rate (Single-ended)

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Single-ended Output Slew Rate (VOH=VDDQ/3)	SRQse	3.5	9	V/ns	1
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-	-

Note:

1. SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: single-ended Signals.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)=0.8*VOH(DC).
5. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Table 8-2 LPDDR4x Output Slew Rate (Single-ended) for 0.6V VDDQ

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Single-ended Output Slew Rate (VOH=VDDQ*0.5)	SRQse	3	9	V/ns	1,2,3,4,5
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-	2,3,4,5

Note:

1. SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: single-ended Signals.
2. Measured with output reference load.

3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)=0.8*VOH(DC).
5. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.2 Differential Output Slew Rate

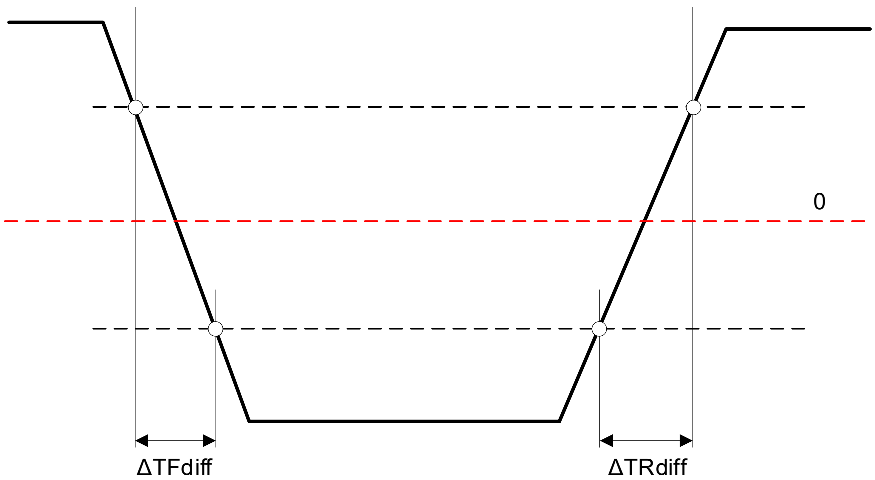


Figure 8-2 Differential Output Slew Rate Definition

Table 8-3 LPDDR4 Differential Output Slew Rate

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Differential Output Slew Rate (VOH=VDDQ/3)	SRQdiff	7	18	V/ns	1,2,3,4

Note:
1. SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: differential Signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=-0.8*VOH(DC) and VOH(AC)=0.8*VOH(DC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

Table 8-4 LPDDR4x Differential Output Slew Rate for 0.6V VDDQ

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Differential Output Slew Rate (VOH=VDDQ*0.5)	SRQdiff	6	18	V/ns	1,2,3,4

Note:
1. SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: differential Signals.
2. Measured with output reference load.

3. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=-0.8*VOH(DC) and VOH(AC)=0.8*VOH(DC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.3 Overshoot and Undershoot for LVSTL

Table 8-5 AC Overshoot/Undershoot Specification

Parameter	Min/Max	Data Rate	Unit
		1600/1866/3200/3733/4266	
Maximum peak amplitude allowed for overshoot area. See Figure 8-3	Max	0.3	V
Maximum peak amplitude allowed for undershoot area. See Figure 8-3	Max	0.3	V
Maximum area above VDD. See Figure 8-3	Max	0.1	V-ns
Maximum area below VSS. See Figure 8-3	Max	0.1	V-ns

Note:

1. VDD stands for VDD2 for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.
2. VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

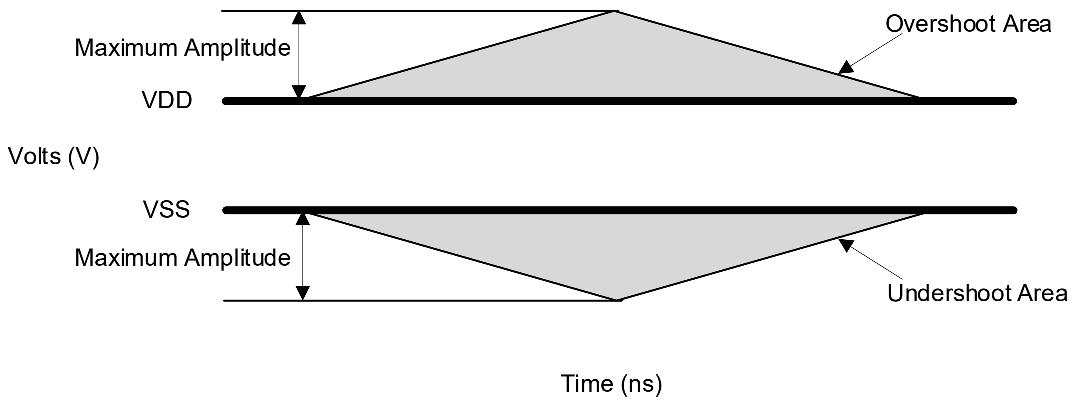


Figure 8-3 Overshoot and Undershoot Definition

8.4 Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

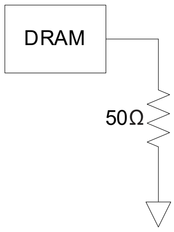


Figure 8-4 Driver Output Reference Load for Timing and Slew Rate

Note:

1. All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

8.5 LVSTL(Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 8-5.

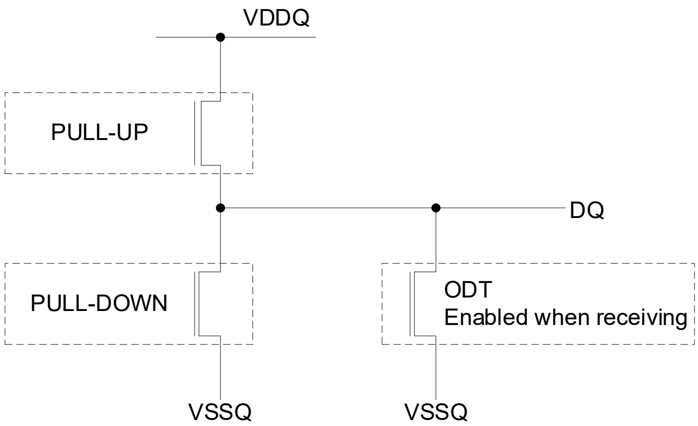


Figure 8-5 LVSTL I/O Cell

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrated as below procedure. First calibrate the pull-down device against a 240Ω resister to VDDQ via the ZQ pin.

- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is less than VDDQ/2.
- NMOS pull-down device is calibrated to 240Ω.

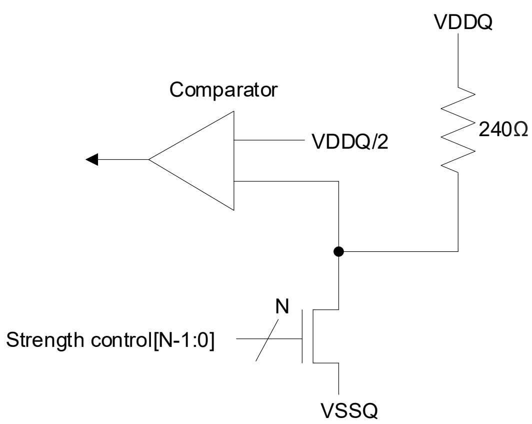


Figure 8-6 Pull-down Calibration

Then calibrate the pull-up device against the calibrated pull-down device.

- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is greater than VOH target.
- NMOS pull-up device is now calibrated to VOH target.

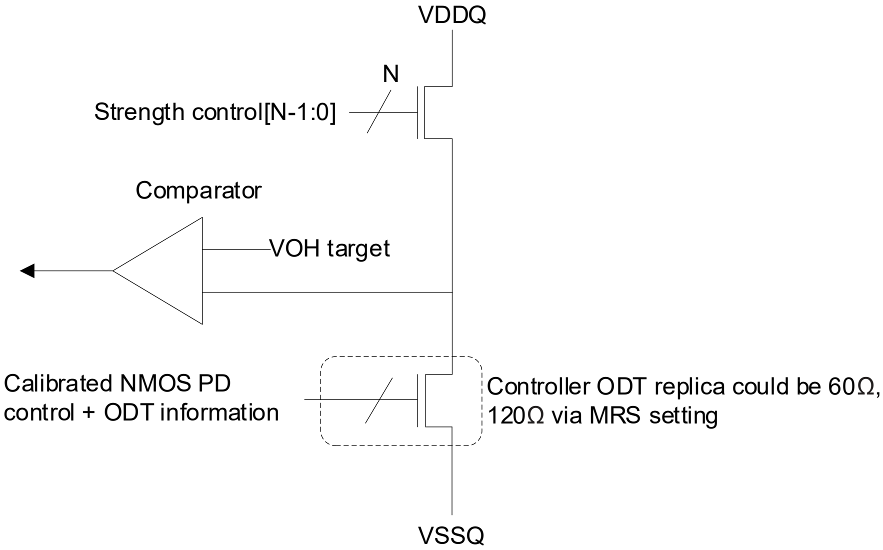


Figure 8-7 Pull-up Calibration

9 IDD Specification Parameters and Test Conditions

9.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: VIN≤VIL(DC) max.

HIGH: VIN≥VIH(DC) min.

STABLE: Inputs are stable at a HIGH or LOW level.

SWITCHING: See Table 9-1 and Table 9-2.

Table 9-1 through Table 9-13 provide the IDD measurement conditions.

Table 9-1 Definition of Switching for CA Input Signals

Switching for CA								
CK_t Edge	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:

1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 9-2 CA Pattern for IDD4R for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:

1. BA[2:0]=010, CA[9:4]=000000 or 111111, Burst Order CA[3:2]=00 or 11 (Same as LPDDR3 IDD4R Spec).
2. Difference from LPDDR3 (JESD209-3): CA pins are kept LOW with DES CMD to reduce ODT current.

Table 9-3 CA Pattern for IDD4W for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

Note:

1. BA[2:0]=010, CA[9:4]=000000 or 111111 (Same as LPDDR3 IDD4W Spec).
2. Difference from LPDDR3 (JESD209-3): 1) No burst ordering, and 2) CA pins are kept LOW with DES CMD to reduce ODT current.

Table 9-4 Data Pattern for IDD4W (DBI off) for BL=16

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16	0	

Note:

1. Simplified pattern compared predecessor. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 9-5 Data Pattern for IDD4R (DBI off) for BL=16

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16	0	

Note:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 9-6 Data Pattern for IDD4W (DBI On) for BL=16

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Note:

1. DBI enabled burst.

Table 9-7 Data Pattern for IDD4R (DBI On) for BL=16

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

Table 9-8 CA Pattern for IDD4R for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note:

1. BA[2:0]=010, CA[9:4]=000000 or 111111, Burst Order CA[4:2]=000 or 111 (Same as LPDDR3 IDD4R Spec).

Table 9-9 CA Pattern for IDD4W for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

Note:

1. BA[2:0]=010, CA[9:5]=00000 or 11111 (Same as LPDDR3 IDD4W Spec).

Table 9-10 Data Pattern for IDD4W (DBI off) for BL=32

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL38	1	1	1	1	1	1	0	0	0	6
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	32	32	32	32	32	32	32	32	0	

Note:

1. Simplified pattern compared predecessor. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 9-11 Data Pattern for IDD4R (DBI off) for BL=32

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	32	32	32	32	32	32	32	32	0	

Note:

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

Table 9-12 Data Pattern for IDD4W (DBI On) for BL=32

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4

	DBI ON Case									No. of 1's
	DQ[7]	**DQ[6]**	**DQ[5]**	**DQ[4]**	**DQ[3]**	**DQ[2]**	**DQ[1]**	**DQ[0]**	**DBI**	
BL38	0	0	0	0	0	0	1	1	1	3
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

Note:

1. DBI enabled burst.

Table 9-13 Data Pattern for IDD4R (DBI On) for BL=32

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4

DBI ON Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

9.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire elevated temperature range. See Table 9-14.

Table 9-14 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Note
Operating one bank active-precharge current: tCK=tCKmin; tRC=tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD01	VDD1	-
	IDD02	VDD2	-
	IDD0Q	VDDQ	3
Idle power-down standby current: tCK=tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2P1	VDD1	-
	IDD2P2	VDD2	-
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD2PS1	VDD1	-
	IDD2PS2	VDD2	-
	IDD2PSQ	VDDQ	3
Idle non-power-down standby current: tCK=tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD2N1	VDD1	-
	IDD2N2	VDD2	-
	IDD2NQ	VDDQ	3
Idle non-power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD2NS1	VDD1	-
	IDD2NS2	VDD2	-
	IDD2NSQ	VDDQ	3
Active power-down standby current: tCK=tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3P1	VDD1	-
	IDD3P2	VDD2	-
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stop: CK_t=LOW, CK_ c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3PS1	VDD1	-
	IDD3PS2	VDD2	-
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: tCK=tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable, ODT disabled	IDD3N1	VDD1	-
	IDD3N2	VDD2	-
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped: CK_ t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable, ODT disabled	IDD3NS1	VDD1	-
	IDD3NS2	VDD2	-
	IDD3NSQ	VDDQ	4
Operating burst READ current: tCK=tCKmin; CS is LOW between valid commands; One bank is active; BL=16 or 32; RL=RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R1	VDD1	-
	IDD4R2	VDD2	-
	IDD4RQ	VDDQ	5
Operating burst WRITE current: tCK=tCKmin; CS is LOW between valid commands; One bank is active; BL=16 or 32; WL=WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W1	VDD1	-
	IDD4W2	VDD2	-
	IDD4WQ	VDDQ	4
	IDD51	VDD1	-

Parameter/Condition	Symbol	Power Supply	Note
All bank REFRESH Burst current: tCK=tCKmin; CKE is HIGH between valid commands; tRC=tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD52	VDD2	-
	IDD5Q	VDDQ	4
All bank REFRESH Average current: tCK=tCKmin; CKE is HIGH between valid commands; tRC=tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD5AB1	VDD1	-
	IDD5AB2	VDD2	-
	IDD5ABQ	VDDQ	4
Per bank REFRESH Average current: tCK=tCKmin; CKE is HIGH between valid commands; tRC=tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	IDD5PB1	VDD1	-
	IDD5PB2	VDD2	-
	IDD5PBQ	VDDQ	4
Power Down Self Refresh current (-25°C to +85°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self Refresh Rate; ODT disabled	IDD61	VDD1	6,7,8,10
	IDD62	VDD2	6,7,8,10
	IDD6Q	VDDQ	4,6,7,8,10
Power Down Self Refresh current (+85°C to +105°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self Refresh Rate; ODT disabled	IDD6ET1	VDD1	7,8,11
	IDD6ET2	VDD2	7,8,11
	IDD6ETQ	VDDQ	4,7,8,11

Note:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0]=000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load=5pF and RON=40Ω.
6. The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9. For all IDD measurements, VIH_CKE=0.8*VDD2, VIL_CKE=0.2*VDD2.
10. IDD6 85°C is guaranteed, IDD6 45°C is typical of the distribution of the arithmetic mean.
11. IDD6ET is a typical value, is sampled only, and is not tested.
12. Dual Channel devices are specified in dual channel operation (both channels operating together).

9.3 LPDDR4 IDD Parameters - Single Die

VDD2=1.06V~1.17V; VDDQ=1.06V~1.17V; VDD1=1.70V~1.95V; TC=–25°C~+85°C

Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
IDD01	VDD1	2.69	2.69	2.69	mA
IDD02	VDD2	53.49	53.49	53.49	mA
IDD0Q	VDDQ	0.12	0.12	0.12	mA
IDD2P1	VDD1	0.33	0.33	0.33	mA
IDD2P2	VDD2	1.69	1.69	1.69	mA
IDD2PQ	VDDQ	0.12	0.12	0.12	mA
IDD2PS1	VDD1	0.33	0.33	0.33	mA
IDD2PS2	VDD2	1.69	1.69	1.69	mA
IDD2PSQ	VDDQ	0.12	0.12	0.12	mA
IDD2N1	VDD1	0.33	0.33	0.33	mA
IDD2N2	VDD2	28.91	28.91	28.91	mA
IDD2NQ	VDDQ	0.12	0.12	0.12	mA
IDD2NS1	VDD1	0.33	0.33	0.33	mA
IDD2NS2	VDD2	23.09	23.09	23.09	mA
IDD2NSQ	VDDQ	0.12	0.12	0.12	mA
IDD3P1	VDD1	0.53	0.53	0.53	mA
IDD3P2	VDD2	11.17	11.17	11.17	mA
IDD3PQ	VDDQ	0.12	0.12	0.12	mA
IDD3PS1	VDD1	0.53	0.53	0.53	mA
IDD3PS2	VDD2	11.17	11.17	11.17	mA
IDD3PSQ	VDDQ	0.12	0.12	0.12	mA
IDD3N1	VDD1	1.06	1.06	1.06	mA
IDD3N2	VDD2	38.82	38.82	38.82	mA
IDD3NQ	VDDQ	0.12	0.12	0.12	mA
IDD3NS1	VDD1	1.06	1.06	1.06	mA
IDD3NS2	VDD2	33	33	33	mA
IDD3NSQ	VDDQ	0.12	0.12	0.12	mA
IDD4W1	VDD1	2.94	3.2	3.48	mA
IDD4W2	VDD2	198.67	225.89	251.42	mA
IDD4WQ	VDDQ	1.45	1.45	1.45	mA
IDD4R1	VDD1	3.39	3.67	4.03	mA
IDD4R2	VDD2	237.39	269.64	301.86	mA
IDD4RQ	VDDQ	95.84	117.23	119.81	mA
IDD51	VDD1	10.41	10.41	10.41	mA
IDD52	VDD2	117.57	117.57	117.57	mA
IDD5Q	VDDQ	0.12	0.12	0.12	mA
IDD5AB1	VDD1	1.07	1.07	1.07	mA
IDD5AB2	VDD2	34.06	34.06	34.06	mA

Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
IDD5ABQ	VDDQ	0.12	0.12	0.12	mA
IDD5PB1	VDD1	1.13	1.13	1.13	mA
IDD5PB2	VDD2	34.49	34.49	34.49	mA
IDD5PBQ	VDDQ	0.12	0.12	0.12	mA

9.4 LPDDR4 IDD6 Parameters - Single Die

VDD2=1.06V~1.17V; VDDQ=1.06V~1.17V; VDD1=1.70V~1.95V; TC=–25°C~+85°C

Temperature	Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
25°C	IDD61	VDD1	0.33	0.33	0.33	mA
	IDD62	VDD2	1.19	1.19	1.19	mA
	IDD6Q	VDDQ	0.12	0.12	0.12	mA
85°C	IDD61	VDD1	0.8	0.8	0.8	mA
	IDD62	VDD2	6.56	6.56	6.56	mA
	IDD6Q	VDDQ	0.12	0.12	0.12	mA

9.5 LPDDR4x IDD Parameters - Single Die

VDD2=1.06V~1.17V; VDDQ=0.57V~0.65V; VDD1=1.70V~1.95V; TC=–25°C~+85°C

Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
IDD01	VDD1	2.69	2.69	2.69	mA
IDD02	VDD2	53.49	53.49	53.49	mA
IDD0Q	VDDQ	0.12	0.12	0.12	mA
IDD2P1	VDD1	0.33	0.33	0.33	mA
IDD2P2	VDD2	1.69	1.69	1.69	mA
IDD2PQ	VDDQ	0.12	0.12	0.12	mA
IDD2PS1	VDD1	0.33	0.33	0.33	mA
IDD2PS2	VDD2	1.69	1.69	1.69	mA
IDD2PSQ	VDDQ	0.12	0.12	0.12	mA
IDD2N1	VDD1	0.33	0.33	0.33	mA
IDD2N2	VDD2	28.91	28.91	28.91	mA
IDD2NQ	VDDQ	0.12	0.12	0.12	mA
IDD2NS1	VDD1	0.33	0.33	0.33	mA
IDD2NS2	VDD2	23.09	23.09	23.09	mA
IDD2NSQ	VDDQ	0.12	0.12	0.12	mA
IDD3P1	VDD1	0.53	0.53	0.53	mA
IDD3P2	VDD2	11.17	11.17	11.17	mA
IDD3PQ	VDDQ	0.12	0.12	0.12	mA
IDD3PS1	VDD1	0.53	0.53	0.53	mA
IDD3PS2	VDD2	11.17	11.17	11.17	mA
IDD3PSQ	VDDQ	0.12	0.12	0.12	mA
IDD3N1	VDD1	1.06	1.06	1.06	mA

Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
IDD3N2	VDD2	38.82	38.82	38.82	mA
IDD3NQ	VDDQ	0.12	0.12	0.12	mA
IDD3NS1	VDD1	1.06	1.06	1.06	mA
IDD3NS2	VDD2	33	33	33	mA
IDD3NSQ	VDDQ	0.12	0.12	0.12	mA
IDD4W1	VDD1	2.94	3.2	3.48	mA
IDD4W2	VDD2	198.67	225.89	251.42	mA
IDD4WQ	VDDQ	1.16	1.16	1.16	mA
IDD4R1	VDD1	3.39	3.67	4.03	mA
IDD4R2	VDD2	237.39	269.64	301.86	mA
IDD4RQ	VDDQ	91.55	93.78	95.84	mA
IDD51	VDD1	10.41	10.41	10.41	mA
IDD52	VDD2	117.57	117.57	117.57	mA
IDD5Q	VDDQ	0.12	0.12	0.12	mA
IDD5AB1	VDD1	1.07	1.07	1.07	mA
IDD5AB2	VDD2	34.06	34.06	34.06	mA
IDD5ABQ	VDDQ	0.12	0.12	0.12	mA
IDD5PB1	VDD1	1.13	1.13	1.13	mA
IDD5PB2	VDD2	34.49	34.49	34.49	mA
IDD5PBQ	VDDQ	0.12	0.12	0.12	mA

9.6 LPDDR4x IDD6 Parameters - Single Die

VDD2=1.06V~1.17V; VDDQ=0.57V~0.65V; VDD1=1.70V~1.95V; TC=–25°C~+85°C

Temperature	Symbol	Supply	3200Mbps	3733Mbps	4266Mbps	Unit
25°C	IDD61	VDD1	0.33	0.33	0.33	mA
	IDD62	VDD2	1.19	1.19	1.19	mA
	IDD6Q	VDDQ	0.12	0.12	0.12	mA
85°C	IDD61	VDD1	0.8	0.8	0.8	mA
	IDD62	VDD2	6.56	6.56	6.56	mA
	IDD6Q	VDDQ	0.12	0.12	0.12	mA

10 Input/Output Capacitance

Table 10-1 Input/output Capacitance

Parameter	Symbol	Min	Max	Unit	Note
Input capacitance, CK_t and CK_c	C_{CK}	0.5	0.9	pF	1,2
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.09	pF	1,2,3
Input capacitance, all other input-only pins	C_{I}	0.5	0.9	pF	1,2,4
Input capacitance delta, all other input-only pins	C_{DI}	-0.1	0.1	pF	1,2,5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C_{IO}	0.7	1.3	pF	1,2,6
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.1	pF	1,2,7
Input/output capacitance delta, DQ, DMI	C_{DIO}	-0.1	0.1	pF	1,2,8
Input/output capacitance, ZQ pin	C_{ZQ}	0	5	pF	1,2

Note:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of C_{CK_t}-C_{CK_c}.
4. C_{I} applies to CS_n, CKE, CA0~CA5.
5. C_{DI}=C_{I}-0.5*(C_{CK_t}+C_{CK_c}).
6. DMI loading matches DQ and DQS.
7. Absolute value of C_{DQS_t}-C_{DQS_c}.
8. C_{DIO}=C_{IO}-Avergae(C_{DQn},C_{DMI},C_{DQS_t},C_{DQS_c}) in byte-lane.

11 Electrical Characteristics and AC Timing

11.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4x device.

11.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg)=(\sum_{j=1}^{N} tCKj)/N \quad N=200$$

Unit ‘tCK(avg)’ represents the actual clock average tCK(avg) of the input clock under operation. Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges. tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

11.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

11.1.2.1 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg)=(\sum_{j=1}^{N} tCHj)/(N*tCK(avg)) \quad N=200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg)=(\sum_{j=1}^{N} tCLj)/(N*tCK(avg)) \quad N=200$$

11.1.2.2 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

11.1.2.3 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per)=Min/Max of {tCKi-tCK(avg) where i=1 to 200}.

tJIT(per), act is the actual clock jitter for a given system.

tJIT(per), allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

11.1.2.4 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc)=Max of |{tCK(i+1)-tCK(i)}|.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

11.2 Clock Timing

Table 11-1 Clock AC Timings

Parameter	Symbol	1600/2400/3200/3733/4266		Unit	Note
		Min	Max		
Clock Timing					
Average High pulse width	tCH(avg)	0.46	0.54	tCK(avg)	-
Average Low pulse width	tCL(avg)	0.46	0.54	tCK(avg)	-
Absolute clock period	tCK(abs)	tCK(avg)min+tJIT(per)min	-	ns	-
Absolute High clock pulse width	tCH(abs)	0.43	0.57	tCK(avg)	-
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	tCK(avg)	-

Parameter	Symbol	1600		2400		3200		3733		4266		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing													
Average clock period	tCK(avg)	1.25	100	0.83	100	0.63	100	0.535	100	0.468	100	ns	-
Clock period jitter	tJIT(per)	-70	70	-50	50	-40	40	-34	34	-30	30	ps	-
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	140	-	100	-	80	-	68	-	60	ps	-

11.3 Temperature Derating for AC Timing

Table 11-2 Temperature Derating AC Timing

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4266		
Temperature Derating					1
DQS output access time from CK_t/CK_c (derated)	tDQSCK	Max	3600	ps	-
RAS-to-CAS delay (derated)	tRCD	Min	tRCD+1.875	ns	-
ACTIVATE-to-ACTIVATE command period (derated)	tRC	Min	tRC+3.75	ns	-
Row active time (derated)	tRAS	Min	tRAS+1.875	ns	-
Row precharge time (derated)	tRP	Min	tRP+1.875	ns	-
Active bank A to active bank B (derated)	tRRD	Min	tRRD+1.875	ns	-

Note:

1. Timing derating applies for operation at 85°C to 105°C.

11.4 CA Rx Voltage and Timing

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in Figure 11-1. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in Figure 11-2. The receiver mask(Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

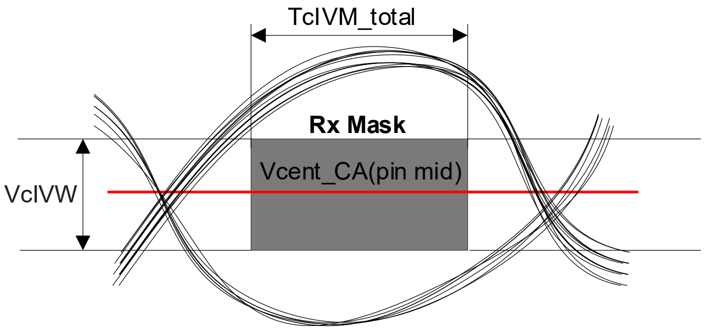


Figure 11-1 CA Receiver(Rx) Mask

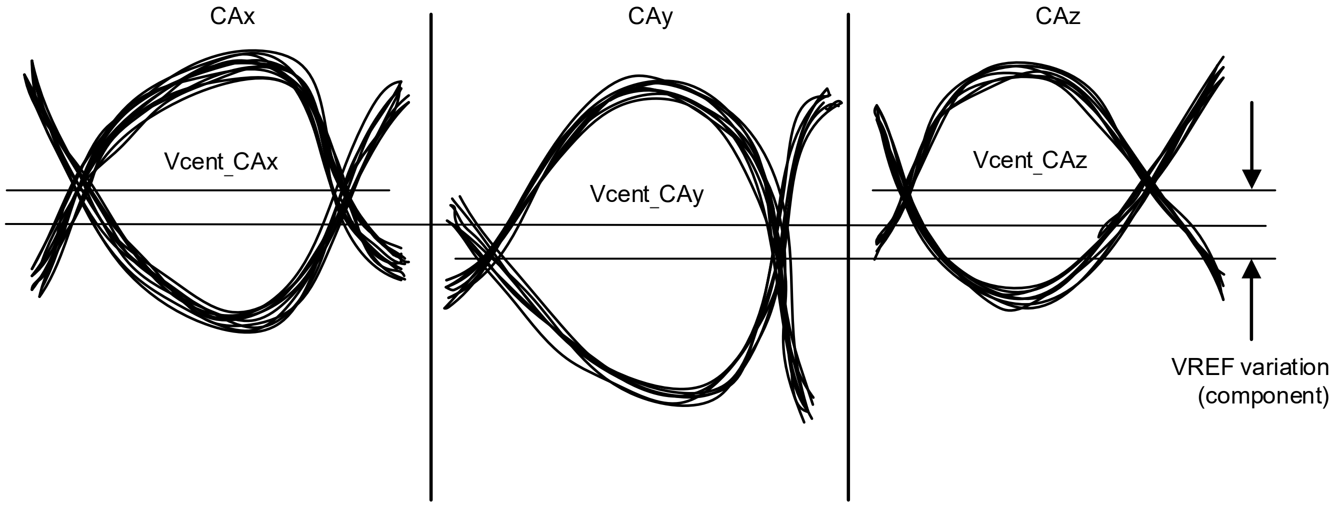


Figure 11-2 Across Pin VREFCA Voltage Variation

Vcent_CA(pin mid) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 11-2. This clarifies that any DRAM component level variation mustbe accounted for within the DRAM CA Rx mask. The component level VREF will be set by the system to account for RON and ODT settings.

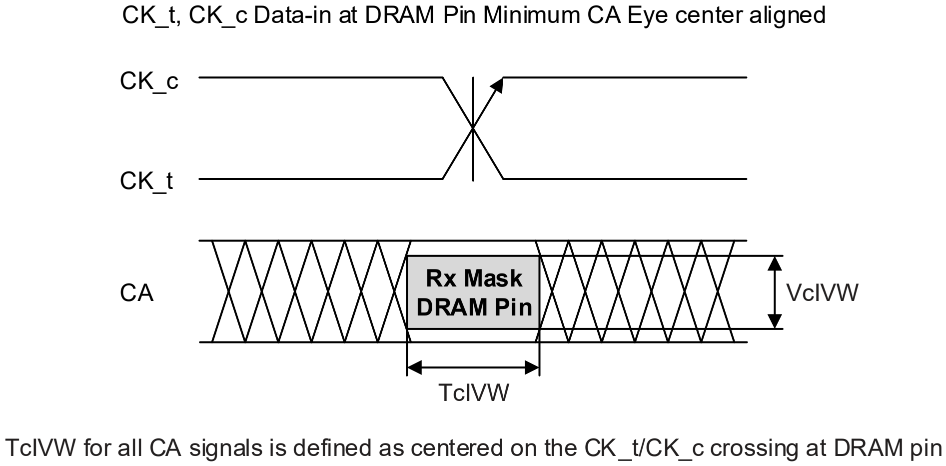


Figure 11-3 CA Timings at the DRAM Pins

All of the timing terms in Table 11-4 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

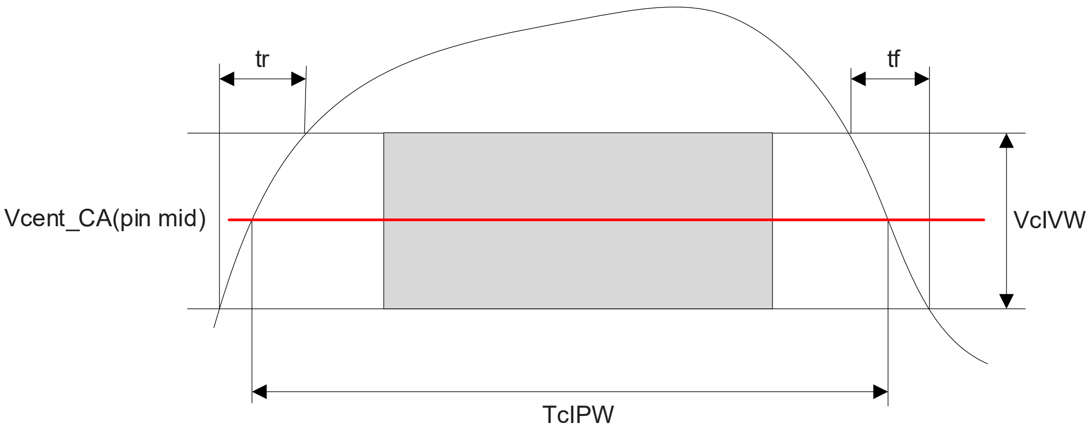


Figure 11-4 CA TcIPW and SRIN_cIVW definition (for each input pulse)

Note:

1. SRIN_cIVW = VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

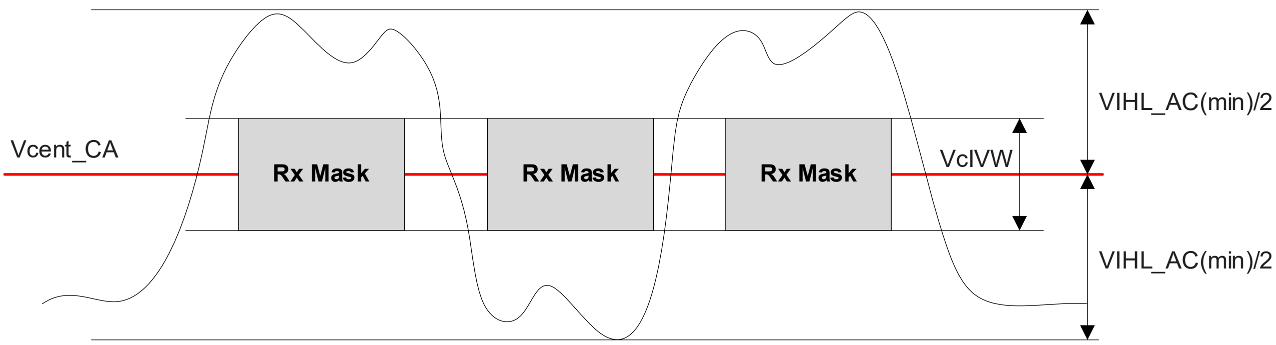


Figure 11-5 CA VIHL(AC) Definition (for Each Input Pulse)

Table 11-3 DRAM CMD/ADR, CS

* UI=tck(avg)min

Symbol	Parameter	DQ-1333/1600/1867		DQ-3200/3733		DQ-4266		Unit	Note
		Min	Max	Min	Max	Min	Max		
VcIVW	Rx Mask voltage peak-peak	-	175	-	155	-	145	mV	2,3,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	UI	2,3,4
VIHL(AC)	CA AC input pulse amplitude peak-peak	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.6		0.6		UI	2,6
SRIN_cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	V/ns	7

Note:

1. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example, the TcIVW(ps) = 450ps at or below 1333 operating frequencies.
2. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
3. Rx mask voltage VcIVW total(Max) must be centered around Vcent_CA(pin mid).
4. Vcent_CA must be within the adjustment range of the CA internal VREF.
5. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL(AC) at any point over the total UI. No timing requirement above level. VIHL(AC) is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL(AC)/2 min must be met both above and below Vcent_CA.
6. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
7. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
8. VIHL(AC) does not have to be met when no transitions are occurring.

11.5 DRAM Data Timing

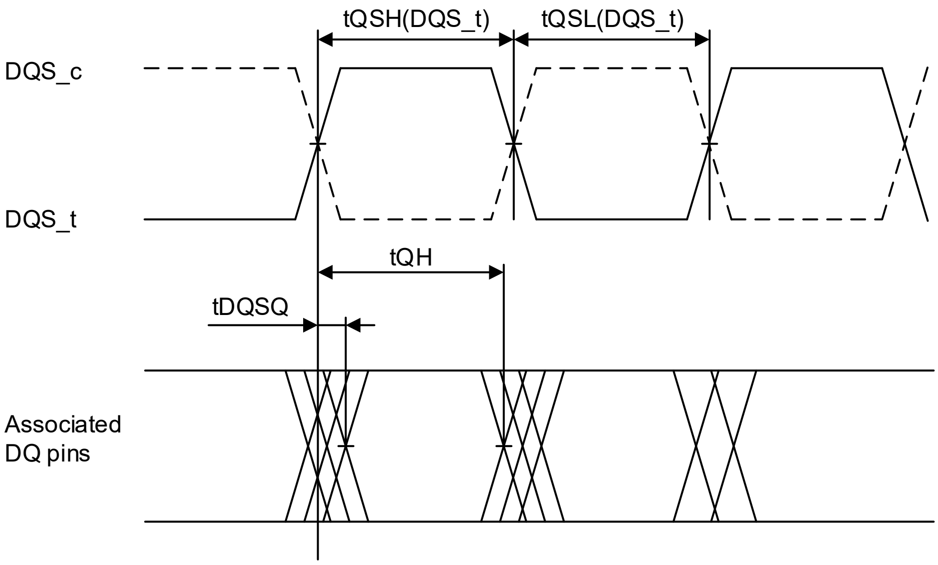


Figure 11-6 Read Data Timing Definitions tQH and tDQSQ across all DQ Signals per DQS Group

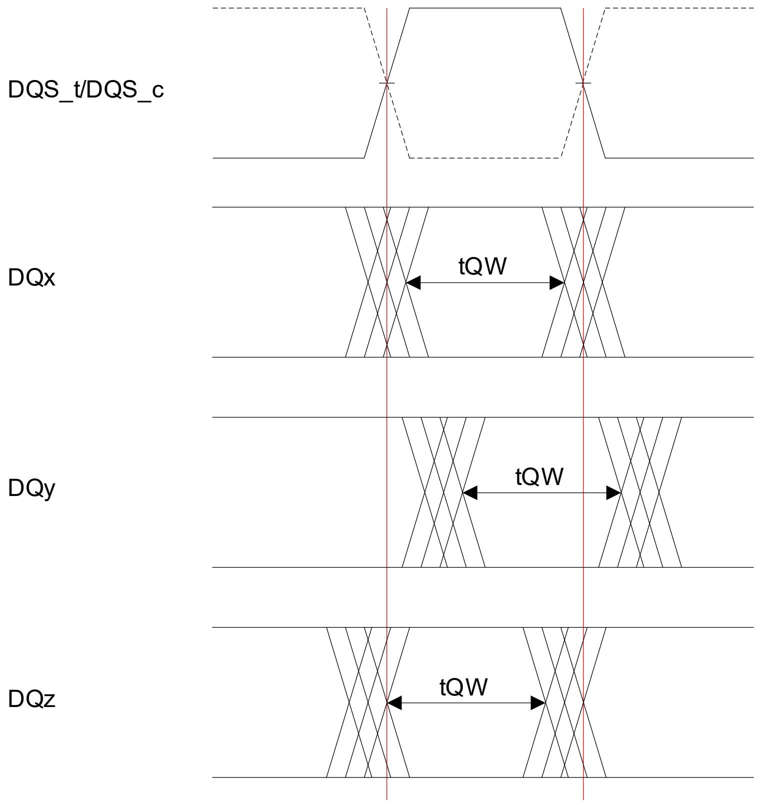


Figure 11-7 Read Data Timing tQW Valid Window Defined per DQ Signal

Table 11-4 Read Output Timings

Unit UI = tCK(avg)min/2

Symbol	Parameter	DQ-1600/1867		DQ-2133/2400		DQ-3200/3733/4266		Unit	Note
		Min	Max	Min	Max	Min	Max		
tDQSQ	DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	-	0.18	-	0.18	-	0.18	UI	-
tQH	DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	Min(tQSH,tQSL)	-	Min(tQSH,tQSL)	-	Min(tQSH,tQSL)	-	UI	-
tQW_total	DQ output window time total, per pin (DBI-Disabled)	0.75	-	0.73	-	0.7	-	UI	3
tQW_dj	DQ output window time deterministic, per pin (DBI-Disabled)	TBD	-	TBD	-	TBD	-	UI	2,3
tDQSQ_DBI	DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	-	0.18	-	0.18	-	0.18	UI	6
tQH_DBI	DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	Min(tQSH_DBI,tQSL_DBI)	-	Min(tQSH_DBI,tQSL_DBI)	-	Min(tQSH_DBI,tQSL_DBI)	-	UI	-
tQW_total_DBI	DQ output window time total, per pin (DBI-Enabled)	0.75	-	0.73	-	0.7	-	UI	3
tQSL	DQS_t, DQS_c differential output LOW time (DBI-Disabled)	tCL(abs)-0.05	-	tCL(abs)-0.05	-	tCL(abs)-0.05	-	tCK(avg)	3,4
tQSH	DQS_t, DQS_c differential output high time (DBI-Disabled)	tCH(abs)-0.05	-	tCH(abs)-0.05	-	tCH(abs)-0.05	-	tCK(avg)	3,5
tQSL_DBI	DQS_t, DQS_c differential output LOW time (DBI-Enabled)	tCL(abs)-0.045	-	tCL(abs)-0.045	-	tCL(abs)-0.045	-	tCK(avg)	4,6
tQSH_DBI	DQS_t, DQS_c differential output high time (DBI-Enabled)	tCH(abs)-0.045	-	tCH(abs)-0.045	-	tCH(abs)-0.045	-	tCK(avg)	5,6

Note:

1. The deterministic component of the total timing. Measurement method tbd.
2. This parameter will be characterized and guaranteed by design.
3. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.
4. tQSL describes the instantaneous differential output low pulse width on DQS_t-DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5. tQSH describes the instantaneous differential output high pulse width on DQS_t-DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tCK(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs)-0.04.
7. The Tx voltage and absolute timing requirements at 1600Mbps apply for all DQ operating frequencies for speed bins which is less than 1600Mbps.

11.6 DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is shown Figure 11-8 is applied per pin. The “total” mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

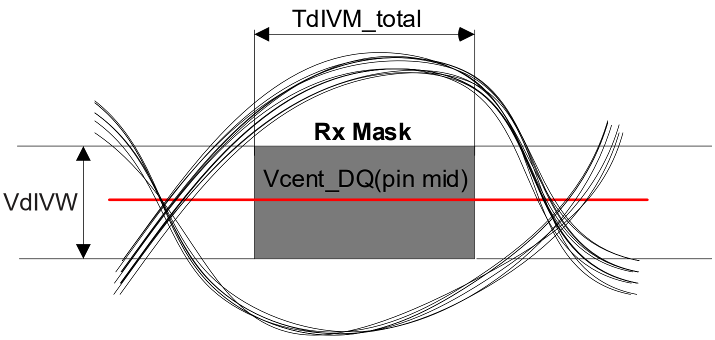


Figure 11-8 DQ Receiver(Rx) Mask

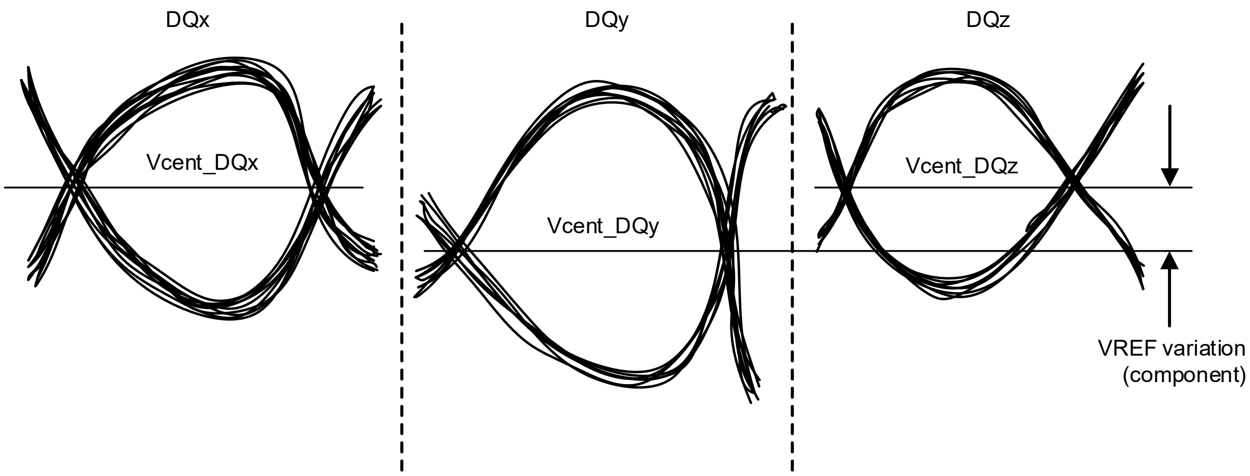


Figure 11-9 Across Pin VREF DQ Voltage Variation

Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depictedin Figure 11-9. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for RON and ODT settings.

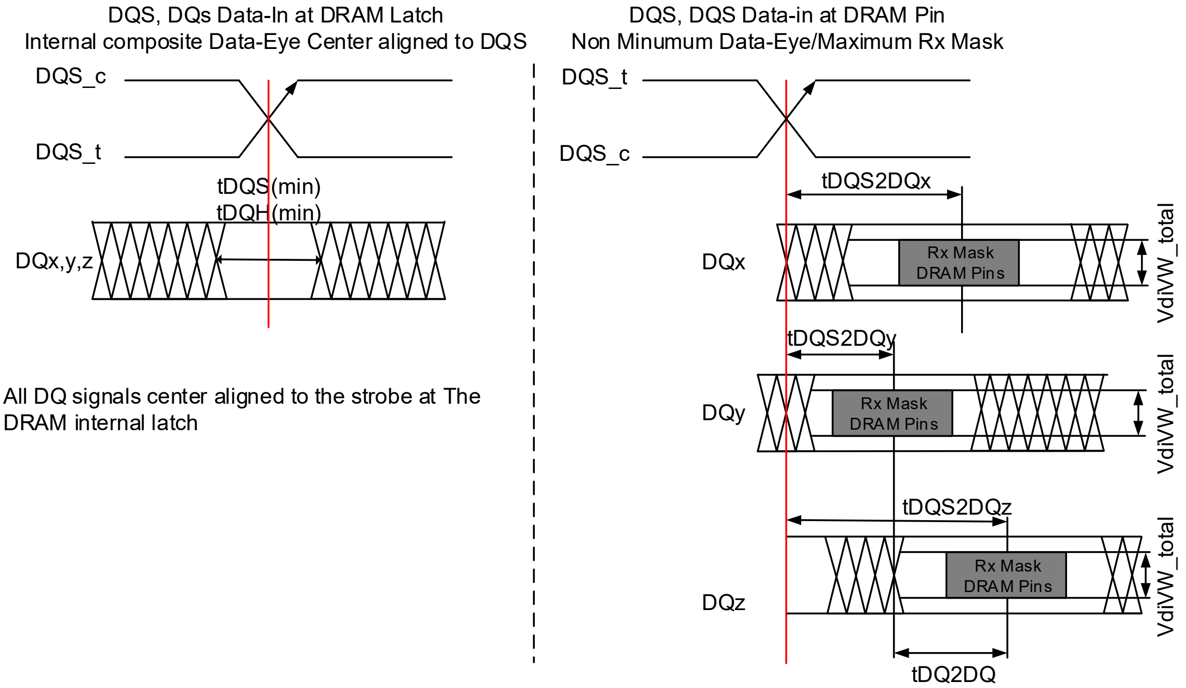


Figure 11-10 **DQ to DQS tDQS2DQ and tDQ2DQ Timings at the DRAM Pins Referenced from the Internal Latch**

Note:

1. The tDQS2DQ is measured at the center(midpoint) of the TdiVW window.
2. The DQz represents the max tDQS2DQ in this example.
3. DQy represents the min tDQS2DQ in this example.

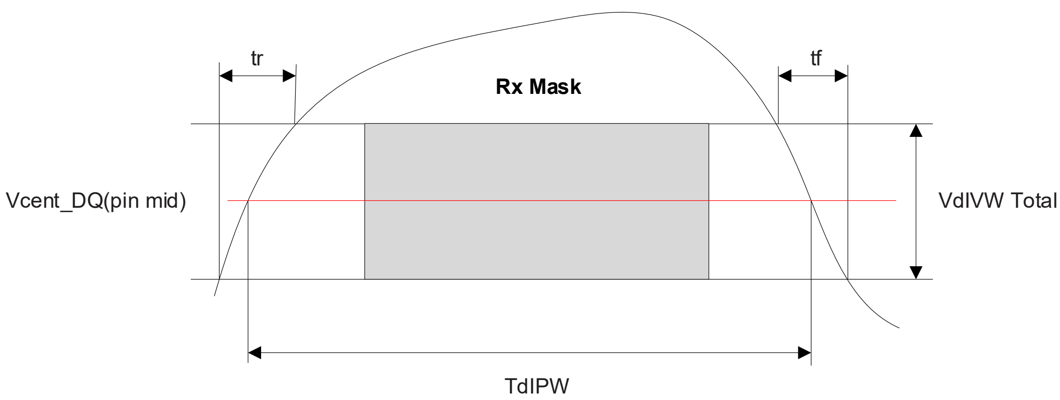


Figure 11-11 DQ TdIPW and SRIN_dIVW Definition (for Each Input Pulse)

Note:

1. SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

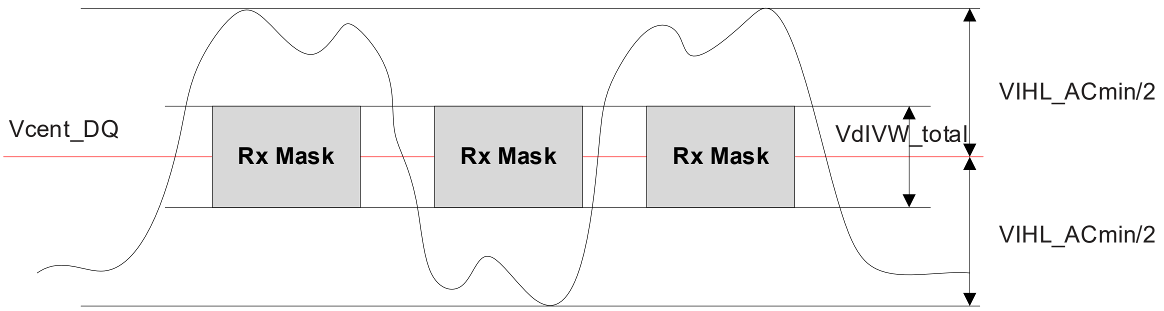


Figure 11-12 DQ VIHL(AC) definition (for Each Input Pulse)

Table 11-5 DRAM DQs in Receive Mode

* UI=tCK(avg)min/2

Symbol	Parameter	DQ-1600/1867/2133/2400		DQ-3200/3733		DQ-4266		Unit	Note
		Min	Max	Min	Max	Min	Max		
VdIVW_total	Rx Mask voltage peak-peak total	-	140	-	140	-	120	mV	2,3,4,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.25	-	0.25	UI	2,3,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	UI	2,3,5,13
VIHL(AC)	DQ AC input pulse amplitude peak-peak	180	-	180	-	170	-	mV	6,14
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45	-	UI	7
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	ps	8
tDQ2DQ	DQ to DQ offset	-	30	-	30	-	30	ps	9
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	ps/°C	10
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	ps/50 mV	11
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	V/ns	12
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	ps	15,16,17

Note:

1. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW_total(ps)=137.5ps at or below 1600 operating frequencies.
2. The Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mV peak-peak from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
3. The design specification is a BER<TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
4. Rx mask voltage VdIVW total(Max) must be centered around Vcent_DQ(pin_mid).
5. Vcent_DQ must be within the adjustment range of the DQ internal VREF.
6. DQ only input pulse amplitude into the receiver must meet or exceed VIHL(AC) at any point over the total UI. No timing requirement above level. VIHL(AC) is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL(AC)/2 min must be met both above and below Vcent_DQ.

7. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
8. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
9. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
10. TDQS2DQ max delay variation as a function of temperature.
11. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies >20MHz and max voltage of 45mV peak-peak from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ=VDD2 is assumed.
12. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
13. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
14. VIHL(AC) does not have to be met when no transitions are occurring.
15. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
16. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
17. tDQS2DQ_rabk2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.

12 AC Timing Parameters

12.1 Core AC Timing

Table 12-1 Core AC Timing Table

Parameter	Symbol	Min/Max	Data Rate		Unit	Note
Core Parameters			**533/1066/1600/2133/2667/3200/3733**	**4266**		
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS+tRPab (with all bank precharge) tRAS+tRPpb (with per bank precharge)		ns	-
Minimum Self Refresh Time (Entry to Exit)	tSR	Min	Max(15ns,3nCK)		ns	-
Self Refresh exit to next valid command delay	tXSR	Min	Max(tRFCab+7.5ns,2nCK)		ns	-
Exit Power-Down to next valid command delay	tXP	Min	Max(7.5ns,5nCK)		ns	-
CAS-to-CAS delay	tCCD	Min	8		tCK(avg)	-
Internal READ to PRECHARGE command delay	tRTP	Min	Max(7.5ns,8nCK)		ns	-
RAS-to-CAS delay	tRCD	Min	Max(18ns,4nCK)		ns	-
Row precharge time (single bank)	tRPpb	Min	Max(18ns,4nCK)		ns	-
Row precharge time (all banks)	tRPab	Min	Max(21ns,4nCK)		ns	-
Row active time	tRAS	Min	Max(42ns,3nCK)		ns	-
Row active time	tRAS	Max	Min(9*tREFI*Refresh Rate,70.2) us (Refresh Rate is specified by MR4, OP [2:0])		us	-
WRITE recovery time	tWR	Min	Max(18ns,6nCK)		ns	-
WRITE-to-READ delay	tWTR	Min	Max(10ns,8nCK)		ns	-
Active bank-A to active bank-B	tRRD	Min	Max(10ns,4nCK)	Max(7.5ns,4nCK)	ns	-
Precharge to Precharge Delay[1]	tPPD	Min	4		tCK	-
Four-bank ACTIVATE window	tFAW	Min	40	30	ns	-

Note:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.

12.2 Read AC Timing

Table 12-2 Read AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Core Parameters			533/1066/1600/2133/2667/3200/3733/4266		
READ preamble	tRPRE	Min	1.8	tCK(avg)	-
0.5 tCK READ postamble	tRPST	Min	0.4	tCK(avg)	-
1.5 tCK READ postamble	tRPST	Min	1.4	tCK(avg)	-
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL*tCK)+tDQSCKmin-200ps	ps	-
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL*tCK)+tDQSCKmax+tDQSQmax+(BL/2*tCK)-100ps	ps	-
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	Min	(RL*tCK)+tDQSCKmin-(tRPREmax*tCK)-200ps	ps	-
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	Max	(RL*tCK)+tDQSCKmax+(BL/2*tCK)+(RPSTmax*tCK)-100ps	ps	-
DQS-DQ skew	tDQSQ	Max	0.18	UI	-

12.3 tDQSCK Timing

Table 12-3 tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Note
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

Note:

1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies >20MHz and max voltage of 45mV peak-peak from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
2. tDQSCK_temp max delay variation as a function of Temperature.
3. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise <20MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise >20MHz. The voltage supply noise must comply to the component Min-Max

DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement VDDQ=VDD2 is assumed.

Table 12-4 CK to DQS Rank to Rank Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Read Timing			**1600/1866/2133/2667/3200/3733/4266**		
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	Max	1	ns	1,2

Note:

1. The same voltage and temperature are applied to tDQS2CK_rank2rank.
2. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

12.4 Write AC Timing

Table 12-5 Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Write Timing			**533/1066/1600/2133/2667/3200/3733/4266**		
Write command to 1st DQS latching	tDQSS	Min	0.75	tCK(avg)	-
		Max	1.25		-
DQS input high-level	tDQSH	Min	0.4	tCK(avg)	
DQS input low-level width	tDQSL	Min	0.4	tCK(avg)	-
DQS falling edge to CK setup time	tDSS	Min	0.2	tCK(avg)	-
DQS falling edge hold time from CK	tDSH	Min	0.2	tCK(avg)	-
Write preamble	tWPRE	Min	1.8	tCK(avg)	-
0.5 tCK Write postamble	tWPST1	Min	0.4	tCK(avg)	1
1.5 tCK Write postamble	tWPST1	Min	1.4	tCK(avg)	1

Note:

1. The length of Write Postamble depends on MR3 OP1 setting.

12.5 Self Refresh Timing

Table 12-6 Self Refresh AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4266		
Self Refresh Timing					
Delay from SRE command to CKE Input LOW	tESCKE	Min	Max (1.75ns, 3tCK)	ns	1
Minimum Self Refresh Time	tSR	Min	Max (15ns, 3tCK)	ns	1
Exit Self Refresh to Valid commands	tXSR	Min	Max (tRFCab+7.5ns, 2tCK)	ns	1

Note:

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 * tCK) and 1.75ns has transpired.

12.6 Mode Register Read/Write AC Timing

Table 12-7 Mode Register Read/Write AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-	-
MODE REGISTER READ command period	tMRR	Min	8	nCK	-
MODE REGISTER WRITE command period	tMRW	Min	Max (10ns, 10nCK)	-	-
Mode register set command delay	tMRD	Min	Max (14ns, 10nCK)	-	-

12.7 VRCG Enable/Disable Timing

Table 12-8 VRCG Enable/Disable Timing Table

Speed		533/1066/1600/2133/2667/3200/3733/4266		Unit
Parameter	Symbol	Min	Max	
VREF high current mode enable time	tVRCG_ENABLE	-	200	ns
VREF high current mode disable time	tVRCG_DISABLE	-	100	ns

12.8 Command Bus Training AC Timing

Table 12-9 Command Bus Training AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
			533/1066/1600/2133/2667/3200/3733/4266		
Command Bus Training Timing					
Valid Clock Requirement after CKE Input LOW	tCKELCK	Min	Max(5ns,5nCK)	-	-
Data Setup for VREF Training Mode	tDStrain	Min	2	ns	-
Data Hold for VREF Training Mode	tDHtrain	Min	2	ns	-
Asynchronous Data Read	tADR	Max	20	ns	-
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)	tCK	2
Valid Strobe Requirement before CKE LOW	tDQSCKE	Min	10	ns	1
First CA Bus Training Command Following CKE LOW	tCAENT	Min	250	ns	-
VREF Step Time-multiple steps	tVREFCA_LONG	Max	250	ns	-
VREF Step Time-one step	tVREFCA_SHORT	Max	80	ns	-
Valid Clock Requirement before CS HIGH	tCKPRECS	Min	2tck+tXP(tXP=Max(7.5ns,5nCK))	-	-
Valid Clock Requirement after CS HIGH	tCKPSTCS	Min	Max(7.5ns,5nCK))	-	-
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2	tCK	-
Minimum delay from CKE HIGH to Strobe HIGH Impedance	tCKEHDQS	Min	10	ns	-
Valid Clock Requirement before CKE Input HIGH	tCKCKEH	Min	Max(1.75ns,3nCK)	-	-

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
CA Bus Training CKE HIGH to DQ Tri-state	tMRZ	Min	1.5	ns	-
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns	-
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns	-
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK,200ns)	-	3
	tXCBT_Middle	Min	Max(5nCK,200ns)	-	3
	tXCBT_Long	Min	Max(5nCK,250ns)	-	3

Note:

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREFCA setting: MR12 OP[5:0] and VREFCA Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 12-18. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREFDQ setting. Settling time of VREFDQ level is same as VREFCA level.

Table 12-10 Command Bus Training AC Timing Table for Mode 1

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
Command Bus Training Timing					
Clock and Command Valid after CKE LOW	tCKELCK	Min	Max(7.5ns,3nCK)	tCK	-
Asynchronous Data Read	tADR	Max	20	ns	-
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)	tCK	1
First CA Bus Training Command Following CKE LOW	tCAENT	Min	250	ns	-
Valid Clock Requirement before CS HIGH	tCKPRECS	Min	2tCK+tXP(tXP=Max(7.5ns,5nCK))		-
Valid Clock Requirement after CS HIGH	tCKPSTCS	Min	Max(7.5ns,5nCK))		-
Clock and Command Valid before CKE HIGH	tCKCKEH	Min	2	tCK	-

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
CA Bus Training CKE HIGH to DQ Tri-state	tMRZ	Min	1.5	ns	-
ODT turn-on Latency from CKE	tCKELODTon	Min	20	ns	-
ODT turn-off Latency from CKE	tCKELODToff	Min	20	ns	-
Exit Command Bus Training	tXCBT_Short	Min	Max(5nCK,200ns)		2
Mode to next valid command delay	tXCBT_Middle	Min	Max(5nCK,200ns)		2
	tXCBT_Long	Min	Max(5nCK,250ns)		2

Note:

1. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
2. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREFCA setting: MR12 OP[5:0] and VREFCA Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREFDQ)setting. Settling time of VREFDQ level is same as VREFCA)level.

Table 12-11 Command Bus Training AC Timing Table for Mode 2

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
Command Bus Training Timing					
Valid Clock Requirement after CKE Input LOW	tCKELCK	Min	Max(5ns,5nCK)	ns	-
Valid Clock Requirement before CS HIGH	tCKPRECS	Min	2tCK+tXP(tXP=Max(7.5ns,5nCK))	-	-
Valid Clock Requirement after CS HIGH	tCKPSTCS	Min	Max(7.5ns,5nCK))	-	-
Valid Strobe Requirement before CKE LOW	tDQSCKE	Min	10	ns	1
First CA Bus Training Command Following CKE LOW	tCAENT	Min	250	ns	-
VREF Step Time - Long	tVREFCA_Long	Max	250	ns	2
VREF Step Time - Middle	tVREFCA_Middle	Max	200	ns	3
VREF Step Time - Short	tVREFCA_Short	Max	100	ns	4
Data Setup for VREF Training Mode	tDStrain	Min	2	ns	-

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
Data Hold for VREF Training Mode	tDHtrain	Min	2	ns	-
Asynchronous Data Read Valid Window	tADVW	Min	16	ns	-
		Max	80	ns	-
DQS Input period at CBT mode	tDQSICYC	Min	5	ns	-
		Max	100	ns	-
Asynchronous Data Read	tADR	Max	20	ns	-
DQS_c high impedance time from CS HIGH	tHZCBT	Min	0	ns	-
Asynchronous Data Read to DQ7 toggle	tAD2DQ7	Min	3	ns	-
		Max	10	ns	-
DQ7sample hold time	tDQ7SH	Min	10	ns	-
		Max	60	ns	-
Asynchronous Data Read Pulse Width	tADSPW	Min	3	ns	-
		Max	10	ns	-
Hi-Z to asynchronous VREFCA valid data	tHZ2VREF	Min	Max(10ns,5nCK)	-	-
Read to Write Delay at CBT mode	tCBTRTW	Min	2	ns	-
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	Max(110ns,4nCK)	-	-
Minimum delay from CKE HIGH to Strobe HIGH Impedance	tCKEHDQS	Min	10	ns	-
Clock and Command Valid before CKE HIGH	tCKCKEH	Min	Max(1.75ns,3nCK)	-	-
ODT turn-on Latency from CKE	tCKELODTon	Max	20	ns	-
ODT turn-off Latency from CKE for ODT_CA	tCKELODToff	Max	20	ns	-
ODT turn-off Latency from CKE for ODT_DQ and DQS	tCKEHODToff	Max	20	ns	-
ODT_DQ turn-off Latency from CS HIGH during CB Training	tODToffCBT	Max	20	ns	-
ODT_DQ turn-on Latency from the end of Valid Data out	tODTonCBT	Max	Max(10ns,5nCK)	-	-
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK,200ns)	-	5

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
	tXCBT_Middle	Min	Max(5nCK,200ns)	-	5
	tXCBT_Long	Min	Max(5nCK,250ns)	-	5

Note:

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. VREFCA_Long is the time including up to VREFmin to VREFmax or VREFmax to VREFmin change across the VREFDQ Range in VREF voltage.
3. VREF_Middle is at least 2 stepsizes increment/decrement change within the same VREFDQ range in VREF voltage.
4. VREF_Short is for a single stepsize increment/decrement change in VREF voltage.
5. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREFCA setting: MR12 OP[5:0] and VREFCA Range: MR12 OP[6] of FSP-OP 0 and 1.

12.9 Frequency Set Point Timing

Table 12-12 Frequency Set Point Timing Table

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
Frequency Set Point parameters					
Frequency Set Point Switching Time	tFC_Short	Min	200	ns	1
Minimum Self Refresh Time	tFC_Middle	Min	200	ns	1
Exit Self Refresh to Valid commands	tFC_Long	Min	250	ns	1
Valid Clock Requirement after Entering FSP Change	tCKFSPE	Min	Max(7.5ns,4nCK)	-	-
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	Min	Max(7.5ns,4nCK)	-	-

Note:

1. Frequency Set Point Switching Time depends on value of VREFCA setting: MR12 OP[5:0] and VREFCA Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally change of Frequency Set Point may affect VREFDQ setting. Settling time of VREFDQ level is same as VREFCA level.

12.10 Write Leveling Timing

Table 12-13 Write Leveling Timing Table

Parameter	Symbol	Min/Max	Value	Unit	Note
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	Min	20	tCK	-
		Max	-		-
Write preamble for Write Leveling	tWLWPRE	Min	20	tCK	-
		Max	-		-
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	Min	40	tCK	-
		Max	-		-
Write leveling output delay	tWLO	Min	0	ns	-
		Max	20		-
Mode register set command delay	tMRD	Min	Max(14ns,10nCK)	ns	-
		Max	-		-
Valid Clock Requirement before DQS Toggle	tCKPRDQS	Min	Max(7.5ns,4nCK)	-	-
		Max	-		-
Valid Clock Requirement after DQS Toggle	tCKPSTDQS	Min	Max(7.5ns,4nCK)	-	-
		Max	-		-

Table 12-14 Write Leveling Setup and Hold Time

Parameter	Symbol	Min/Max	Data Rate					Unit	Note
			1600	2400	3200	3733	4266		
Write Leveling Parameters									
Write leveling hold time	tWLH	Min	150	100	75	62.5	50	ps	-
Write leveling setup time	tWLS	Min	150	100	75	62.5	50	ps	-
Write leveling input valid window	tWLIVW	Min	240	160	120	105	90	ps	-

12.11 MPC [Write FIFO] AC Timing

Table 12-15 MPC [Write FIFO] AC Timing Table

Parameter	Symbol	Min/Max	Data Rate	Note
			533/1066/1600/2133/2667/3200/3733/4266	
MPC Write FIFO Timing				
Additional time after tXP has expired until MPC [Write FIFO] command may be issued	tMPCWR	Min	tRCD+3nCK	-

12.12 DQS Interval Oscillator AC Timing

Table 12-16 DQS Interval Oscillator AC Timing Table

Parameter	Symbol	Min/Max	Value	Unit	Note
Delay time from OSC stop to Mode Register Readout	tOSCO	Min	Max(40ns,8nCK)	ns	-

Note:

1. Start DQS OSC command is prohibited until tOSCOmin is satisfied.

12.13 Read Preamble Training Timing

Table 12-17 Read Preamble Training Timing Table

Parameter	Symbol	Min	Max	Note
Delay from MRW command to DQS Driven	tSDO	-	Max(12nCK,20ns)	-

12.14 ZQ Calibration Timing

Table 12-18 ZQCal Timing Table

Parameter	Symbol	Min /Max	Value	Unit	Note
ZQ Calibration Time	tZQCAL	Min	1	us	-
ZQ Calibration Latch Time	tZQLAT	Min	Max(30ns,8nCK)	ns	-
ZQ Calibration Reset Time	tZQRESET	Min	Max(50ns,3nCK)	ns	-

12.15 ODT CA AC Timing

Table 12-19 ODT CA AC Timing Table

Speed		1600/1866/2133/2400/3200/3733/4266		Note
Parameter	Symbol	Min	Max	
ODT CA Value Update Time	tODTUP	RU (20ns/tCK(avg))	-	-

12.16 Power-Down AC Timing

Table 12-20 Power-Down AC Timing

Parameter	Symbol	Min/Max	Data Rate 533/1066/1600/2133/2667/3200/3733/4266	Unit	Note
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width) tCKE	tCKE	Min	Max (7.5ns, 4nCK)	-	-
Delay from valid command to CKE Input LOW	tCMDCKE	Min	Max (1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input LOW	tCKELCK	Min	Max (5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input LOW	tCSCKE	Min	1.75	ns	-
Valid CS Requirement after CKE Input LOW	tCKELCS	Min	Max (5ns, 5nCK)	ns	-
Valid Clock Requirement before CKE Input HIGH	tCKCKEH	Min	Max (1.75ns, 3nCK)	ns	1
Exit power-down to next valid command delay	tXP	Min	Max (7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input HIGH	tCSCKEH	Min	1.75	ns	-
Valid CS Requirement after CKE Input HGIH	tCKEHCS	Min	Max (7.5ns, 5nCK)	ns	-
Valid Clock and CS Requirement after CKE Input LOW after MRW Command	tMRWCKEL	Min	Max (14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input LOW after ZQ Calibration Start Command	tZQCKE	Min	Max (1.75ns, 3nCK)	ns	1

Note:

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).

13 Revision History

Version No	Description	Page	Date
1.0	Initial release	---	2025/3/4
1.1	Add Chapter 3 “Simplified LPDDR4 State Diagram” and Chapter 4 “Mode Registers”	12~15	2025/4/30

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